



Q77H2-AD

Rev : 1.0.

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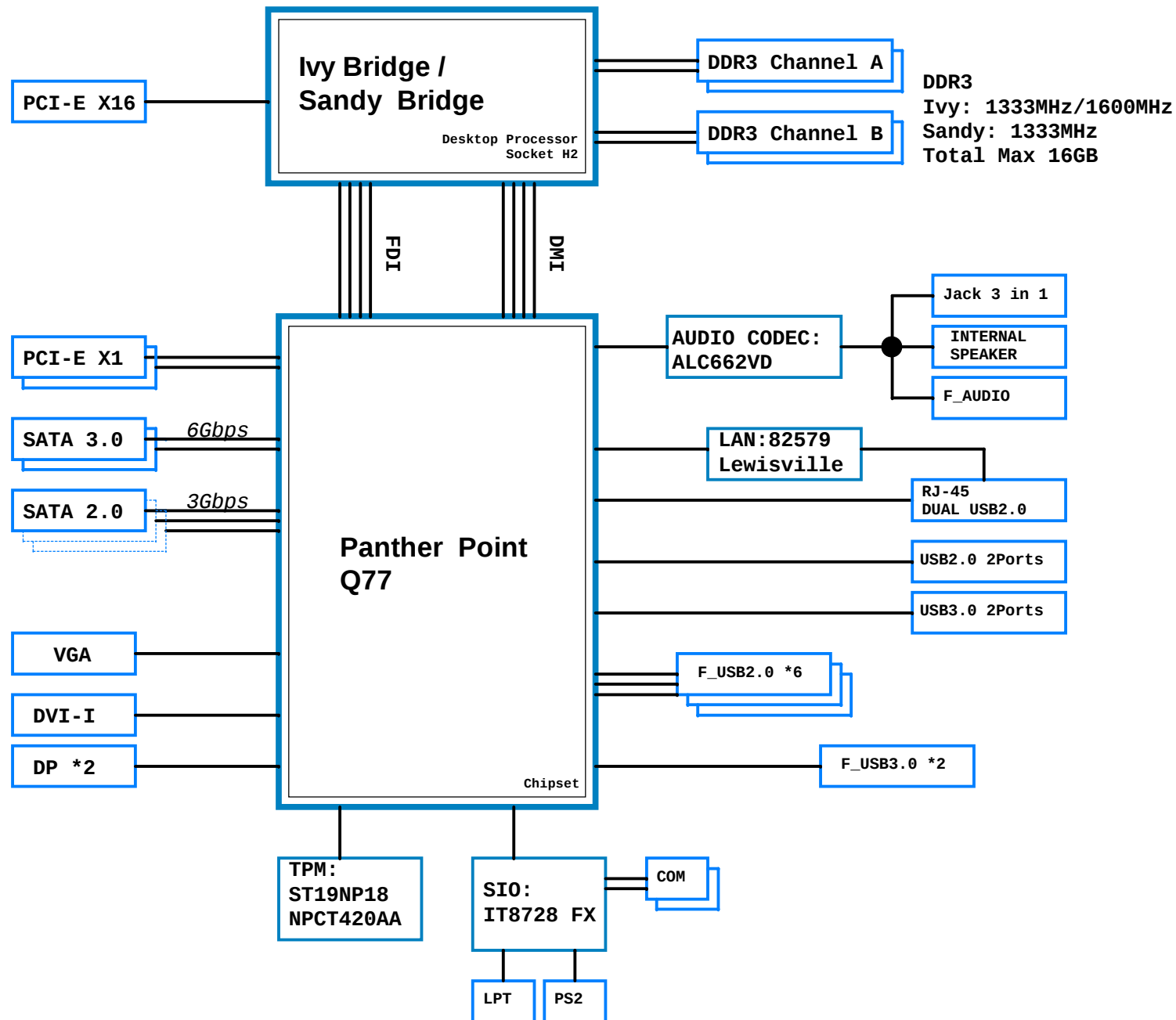
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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version
V.B	2011/12/13	
V1.0	2012/01/17	
V1.0.	2012/04/10	

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GPIO Table

PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO27	I/O	SB_3VSB	Input	LANWAKEB for Bcm
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4S5

IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

Straping Table

PCH Straping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
* H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)	
* H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
* H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
* H	1.5V
L	1.8V

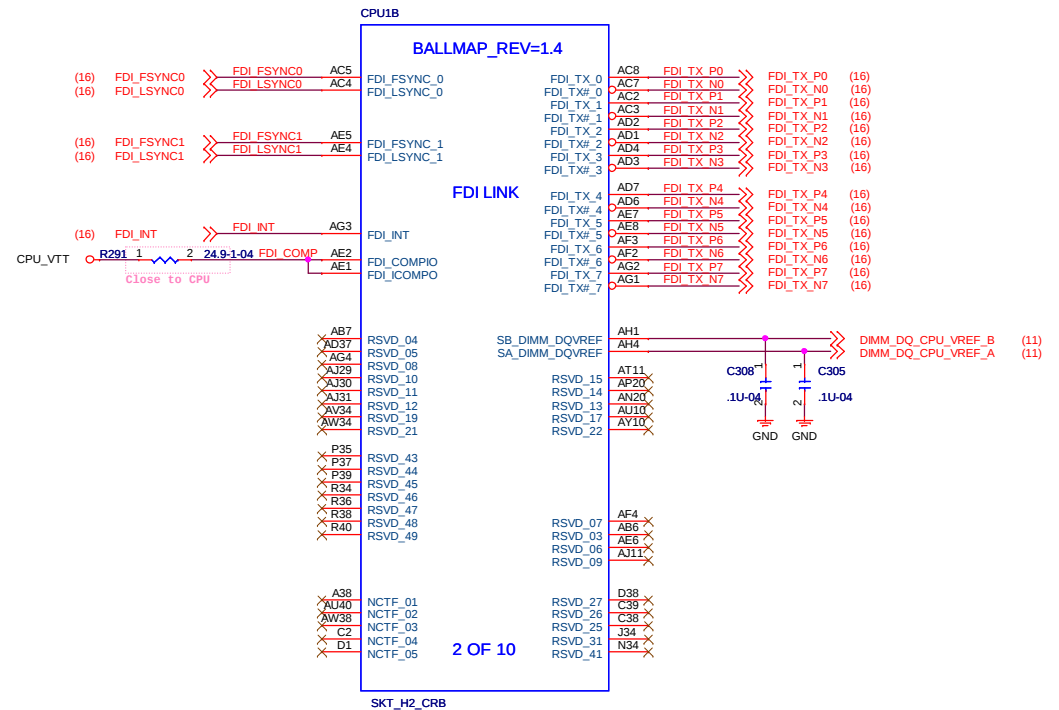
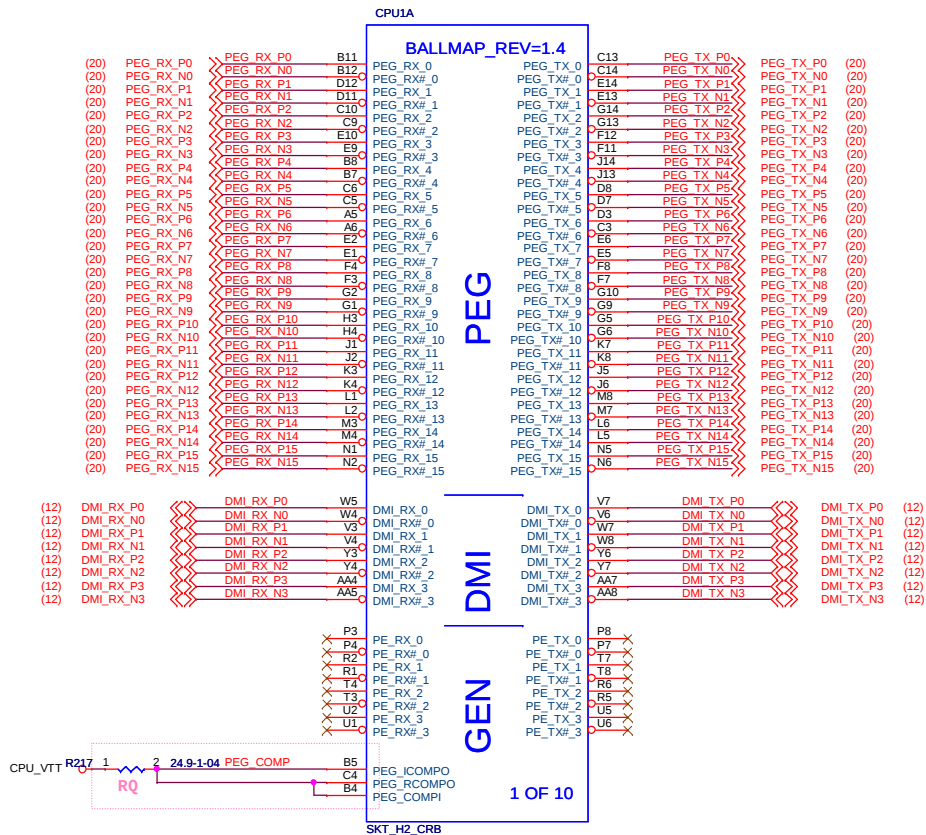
Integrated 1.05V SUS VRM:

INTVRMEN	
* H	Enable
L	Disable

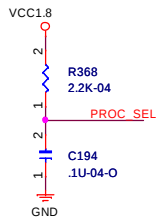
SIO IT8728F D/EX Straping (Page.28)

Power-On Strapping

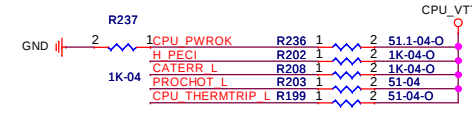
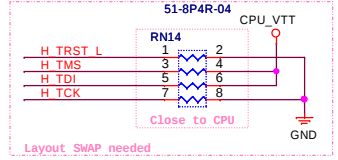
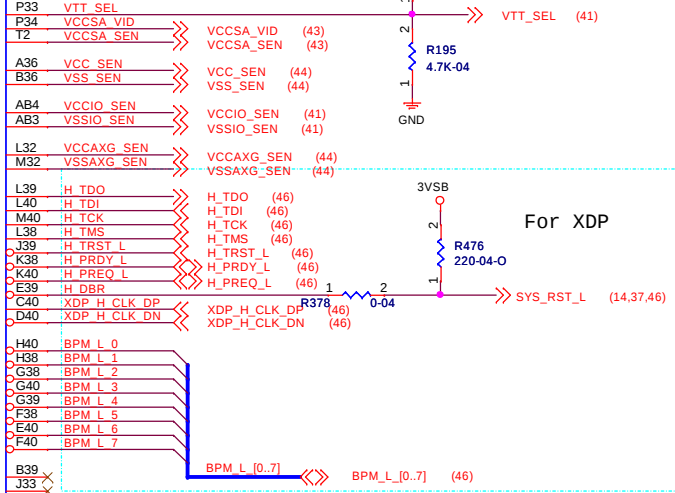
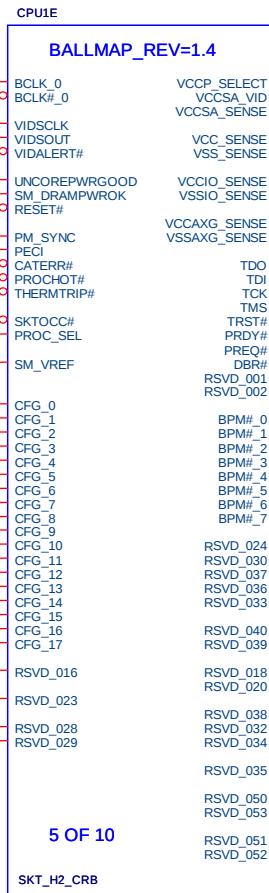
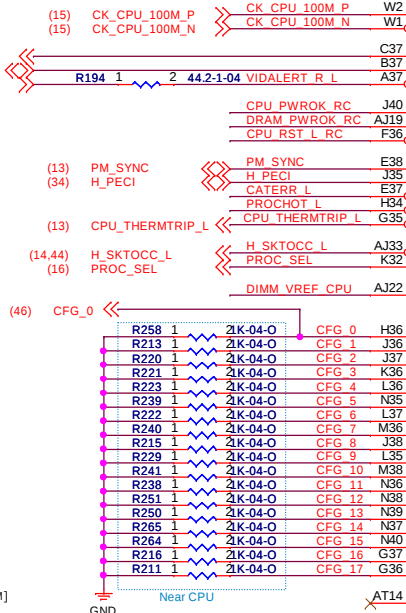
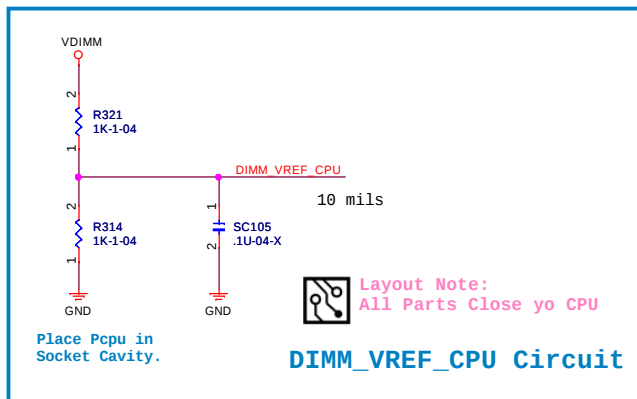
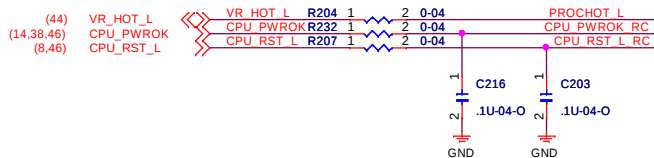
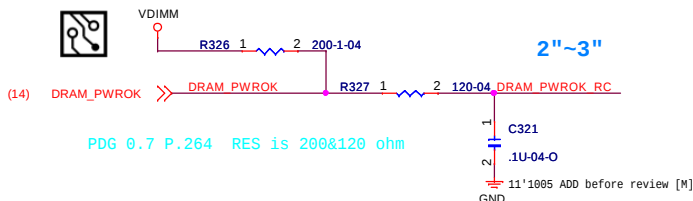
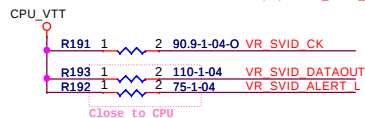
	Symbol	Value	Description
JP1 Pin-48	DSW_EUP_SEL	1 0	EUP DSW
JP2 Pin-122	WDT_EN	1 0	Disable WDT to reset PWR0K Enable WDT to reset PWR0K
JP3 Pin-124	FAN_CTL_SEL	1 0	EC Index 63h/6Bh/73h is 80h EC Index 63h/6Bh/73h is 00h
JP4 Pin-126	K8PWR_EN	1 0	Disable K8 Power Sequence Enable K8 Power Sequence
JP5 Pin-29	UOVMODE_SEL	1 0	Notice Mode (Default) Force Mode



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

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Title: **CPU - MISC**

Size Custom: **Q77H2-AD**

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CFG_0..17 HAVE INTERNAL PULL-UPS

(9)	M_DATA_A[0..63]	←	M_DATA A[0..63]
(9)	M_DQS_A_P[0..7]	←	M DQS A P[0..7]
(9)	M_DQS_A_N[0..7]	←	M DQS A N[0..7]
(9)	M_MA_A[0..15]	←	M MA A[0..15]
(9)	M_BS_A[0..2]	←	M BS A[0..2]
(9)	M_CS_A_L[0..3]	←	M CS A L[0..3]
(9)	M_CKE_A[0..3]	←	M CKE A[0..3]
(9)	M_ODT_A[0..3]	←	M ODT A[0..3]
(9)	M_CLK_A_P[0..3]	←	M CLK A P[0..3]
(9)	M_CLK_A_N[0..3]	←	M CLK A N[0..3]
(9)	M_WE_A_L	←	M WE A L
(9)	M_CAS_A_L	←	M CAS A L
(9)	M_RAS_A_L	←	M RAS A L

DDR3 CH.A

(9,10) DDR3_DRAMRST_L ← DDR3_DRAMRST_L

(10)	M_DATA_B[0..63]	←	M_DATA B[0..63]
(10)	M_DQS_B_P[0..7]	←	M DQS B P[0..7]
(10)	M_DQS_B_N[0..7]	←	M DQS B N[0..7]
(10)	M_MA_B[0..15]	←	M MA B[0..15]
(10)	M_BS_B[0..2]	←	M BS B[0..2]
(10)	M_CS_B_L[0..3]	←	M CS B L[0..3]
(10)	M_CKE_B[0..3]	←	M CKE B[0..3]
(10)	M_ODT_B[0..3]	←	M ODT B[0..3]
(10)	M_CLK_B_P[0..3]	←	M CLK B P[0..3]
(10)	M_CLK_B_N[0..3]	←	M CLK B N[0..3]
(10)	M_WE_B_L	←	M WE B L
(10)	M_CAS_B_L	←	M CAS B L
(10)	M_RAS_B_L	←	M RAS B L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_DQ_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AL1	SA_DQ_7
M_DATA_A8	AN1	SA_DQ_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AN2	SA_DQ_12
M_DATA_A13	AN3	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AV3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AW5	SA_DQ_19
M_DATA_A20	AU2	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AY7	SA_DQ_23
M_DATA_A24	AY7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AV7	SA_DQ_29
M_DATA_A30	AW9	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AU36	SA_DQ_35
M_DATA_A36	AW35	SA_DQ_36
M_DATA_A37	AY36	SA_DQ_37
M_DATA_A38	AU38	SA_DQ_38
M_DATA_A39	AW37	SA_DQ_39
M_DATA_A40	AR40	SA_DQ_40
M_DATA_A41	AR37	SA_DQ_41
M_DATA_A42	AN38	SA_DQ_42
M_DATA_A43	AN37	SA_DQ_43
M_DATA_A44	AR39	SA_DQ_44
M_DATA_A45	AR38	SA_DQ_45
M_DATA_A46	AR39	SA_DQ_46
M_DATA_A47	AN40	SA_DQ_47
M_DATA_A48	AL40	SA_DQ_48
M_DATA_A49	AL37	SA_DQ_49
M_DATA_A50	AJ38	SA_DQ_50
M_DATA_A51	AJ37	SA_DQ_51
M_DATA_A52	AL39	SA_DQ_52
M_DATA_A53	AL38	SA_DQ_53
M_DATA_A54	AJ39	SA_DQ_54
M_DATA_A55	AJ40	SA_DQ_55
M_DATA_A56	AG40	SA_DQ_56
M_DATA_A57	AG37	SA_DQ_57
M_DATA_A58	AE38	SA_DQ_58
M_DATA_A59	AE37	SA_DQ_59
M_DATA_A60	AG39	SA_DQ_60
M_DATA_A61	AG38	SA_DQ_61
M_DATA_A62	AE39	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW6	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
SA_ECC_CB_3
SA_ECC_CB_4
SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0
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DDR3 CH.A

BALLMAP_REV=1.4

AV27	M_MA_A0
AY24	M_MA_A1
AW24	M_MA_A2
AW23	M_MA_A3
AV23	M_MA_A4
AT24	M_MA_A5
AT23	M_MA_A6
AU22	M_MA_A7
AV22	M_MA_A8
AT22	M_MA_A9
AV28	M_MA_A10
AU21	M_MA_A11
AT21	M_MA_A12
AW32	M_MA_A13
AU20	M_MA_A14
AT20	M_MA_A15
AW29	M_WE_A_L
AY30	M_CAS_A_L
AU28	M_RAS_A_L
AV29	M_BS_A0
AW28	M_BS_A1
AV20	M_BS_A2
AV29	M_CS_A_L0
AU29	M_CS_A_L1
AW30	M_CS_A_L2
AU33	M_CS_A_L3
AV19	M_CKE_A0
AT19	M_CKE_A1
AU18	M_CKE_A2
AV18	M_CKE_A3
AV31	M_ODT_A0
AU32	M_ODT_A1
AU30	M_ODT_A2
AW33	M_ODT_A3
AY25	M_CLK_A_P0
AW25	M_CLK_A_N0
AU25	M_CLK_A_P1
AW27	M_CLK_A_P2
AY27	M_CLK_A_N2
AV26	M_CLK_A_P3
AW26	M_CLK_A_N3

SA_CK_0
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SA_CK#_1
SA_CK_2
SA_CK#_2
SA_CK_3
SA_CK#_3

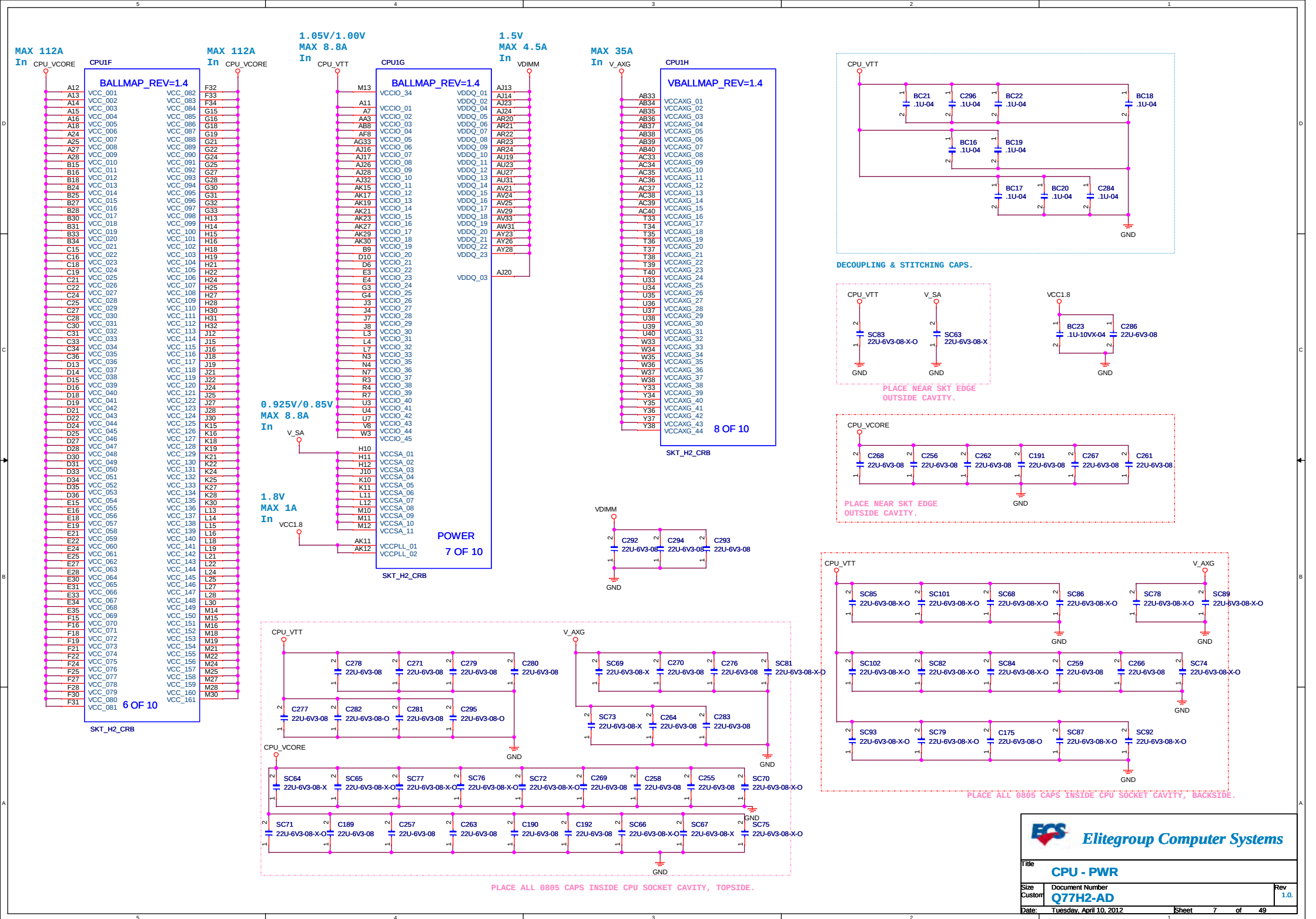
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SA_CKE_3

SA_ODT_0
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SA_ODT_2
SA_ODT_3

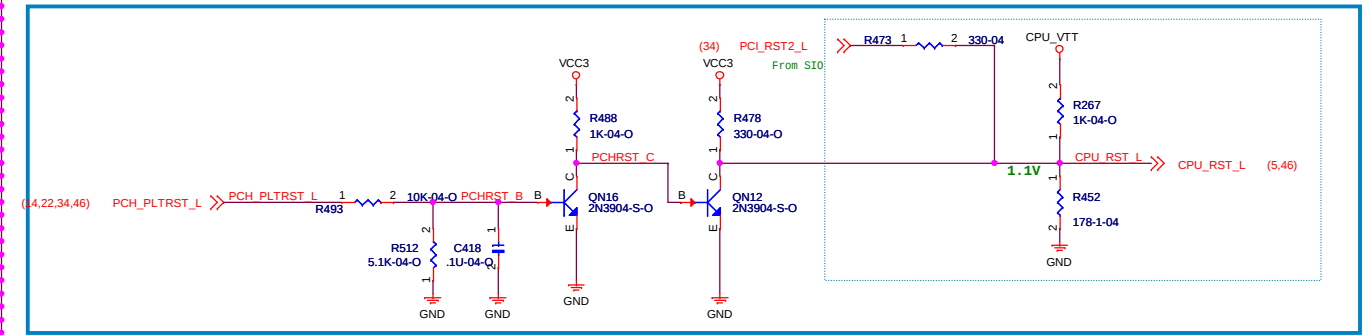
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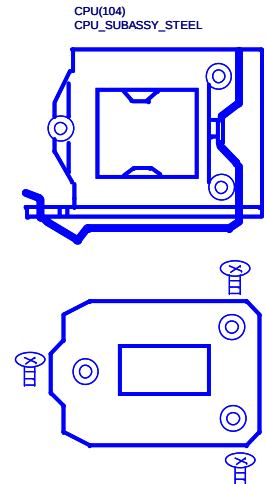
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A23	VSS_002	AM30	AV14	VSS_182	VSS_272
A26	VSS_003	AM36	AV17	VSS_183	VSS_273
A29	VSS_004	AM37	AV3	VSS_184	VSS_274
A35	VSS_005	AM38	AV35	VSS_185	VSS_275
AA33	VSS_006	AM39	AV38	VSS_186	VSS_276
AA34	VSS_007	AM40	AV6	VSS_187	VSS_277
AA35	VSS_008	AM41	AW10	VSS_188	VSS_278
AA36	VSS_009	AM42	AW11	VSS_189	VSS_279
AA37	VSS_010	AM43	AW14	VSS_190	VSS_280
AA38	VSS_011	AM44	AW16	VSS_191	VSS_281
AA6	VSS_012	AM45	AW36	VSS_192	VSS_282
AB5	VSS_013	AM46	AW6	VSS_193	VSS_283
AC1	VSS_014	AM47	AY11	VSS_194	VSS_284
AC6	VSS_015	AM48	AY14	VSS_195	VSS_285
AD33	VSS_016	AM49	AY18	VSS_196	VSS_286
AD36	VSS_017	AM50	AY35	VSS_197	VSS_287
AD38	VSS_018	AM51	AY4	VSS_198	VSS_288
AD39	VSS_019	AM52	AY6	VSS_199	VSS_289
AD40	VSS_020	AM53	AY8	VSS_200	VSS_290
AD5	VSS_021	AM54	B10	VSS_201	VSS_291
AD6	VSS_022	AM55	B13	VSS_202	VSS_292
AE3	VSS_023	AM56	B14	VSS_203	VSS_293
AE33	VSS_024	AM57	B17	VSS_204	VSS_294
AE36	VSS_025	AM58	B23	VSS_205	VSS_295
AF1	VSS_026	AM59	B26	VSS_206	VSS_296
AF34	VSS_027	AM60	B29	VSS_207	VSS_297
AF36	VSS_028	AM61	B32	VSS_208	VSS_298
AF37	VSS_029	AM62	B35	VSS_209	VSS_299
AF40	VSS_030	AM63	B38	VSS_210	VSS_300
AF5	VSS_031	AM64	B6	VSS_211	VSS_301
AF6	VSS_032	AM65	AP11	VSS_212	VSS_302
AF7	VSS_033	AM66	C11	VSS_213	VSS_303
AG36	VSS_034	AM67	C17	VSS_214	VSS_304
AH2	VSS_035	AM68	C20	VSS_215	VSS_305
AH3	VSS_036	AM69	C23	VSS_216	VSS_306
AH33	VSS_037	AM70	C26	VSS_217	VSS_307
AH36	VSS_038	AM71	C29	VSS_218	VSS_308
AH37	VSS_039	AM72	C32	VSS_219	VSS_309
AH38	VSS_040	AM73	C35	VSS_220	VSS_310
AH39	VSS_041	AM74	C7	VSS_221	VSS_311
AH40	VSS_042	AM75	AP40	VSS_222	VSS_312
AH5	VSS_043	AM76	AP5	VSS_223	VSS_313
AH6	VSS_044	AM77	AR11	VSS_224	VSS_314
AJ12	VSS_045	AM78	AR14	VSS_225	VSS_315
AJ15	VSS_046	AM79	AR17	VSS_226	VSS_316
AJ18	VSS_047	AM80	AR18	VSS_227	VSS_317
AJ21	VSS_048	AM81	AR19	VSS_228	VSS_318
AJ25	VSS_049	AM82	AR27	VSS_229	VSS_319
AJ27	VSS_050	AM83	AR30	VSS_230	VSS_320
AJ36	VSS_051	AM84	AR36	VSS_231	VSS_321
AJ5	VSS_052	AM85	AR5	VSS_232	VSS_322
AK1	VSS_053	AM86	AT1	VSS_233	VSS_323
AK10	VSS_054	AM87	AT10	VSS_234	VSS_324
AK13	VSS_055	AM88	AT12	VSS_235	VSS_325
AK14	VSS_056	AM89	AT13	VSS_236	VSS_326
AK16	VSS_057	AM90	AT15	VSS_237	VSS_327
AK22	VSS_058	AM91	AT16	VSS_238	VSS_328
AK28	VSS_059	AM92	AT17	VSS_239	VSS_329
AK31	VSS_060	AM93	AT2	VSS_240	VSS_330
AK32	VSS_061	AM94	AT25	VSS_241	VSS_331
AK33	VSS_062	AM95	AT27	VSS_242	VSS_332
AK34	VSS_063	AM96	AT28	VSS_243	VSS_333
AK35	VSS_064	AM97	AT29	VSS_244	VSS_334
AK36	VSS_065	AM98	AT3	VSS_245	VSS_335
AK37	VSS_066	AM99	AT30	VSS_246	VSS_336
AK4	VSS_067	AM100	AT31	VSS_247	VSS_337
AK40	VSS_068	AM101	AT32	VSS_248	VSS_338
AK5	VSS_069	AM102	AT33	VSS_249	VSS_339
AK6	VSS_070	AM103	AT34	VSS_250	VSS_340
AK7	VSS_071	AM104	AT35	VSS_251	VSS_341
AK8	VSS_072	AM105	AT36	VSS_252	VSS_342
AK9	VSS_073	AM106	AT37	VSS_253	VSS_343
AL11	VSS_074	AM107	AT38	VSS_254	VSS_344
AL14	VSS_075	AM108	AT39	VSS_255	VSS_345
AL17	VSS_076	AM109	AT4	VSS_256	VSS_346
AL19	VSS_077	AM110	AT40	VSS_257	VSS_347
AL24	VSS_078	AM111	F37	VSS_258	VSS_348
AL27	VSS_079	AM112	F39	VSS_259	VSS_349
AL30	VSS_080	AM113	F5	VSS_260	VSS_350
AL36	VSS_081	AM114	F6	VSS_261	VSS_351
AL5	VSS_082	AM115	F9	VSS_262	VSS_352
AM1	VSS_083	AM116	G11	VSS_263	VSS_353
AM11	VSS_084	AM117	G12	VSS_264	VSS_354
AM14	VSS_085	AM118	G17	VSS_265	VSS_355
AM17	VSS_086	AM119	G20	VSS_266	VSS_356
AM2	VSS_087	AM120	G23	VSS_267	VSS_357
AM21	VSS_088	AM121	G26	VSS_268	VSS_358
AM23	VSS_089	AM122	G29	VSS_269	VSS_359
AM25	VSS_090	AM123	G34	VSS_270	VSS_360
AM25	VSS_090	AM124	G7	VSS_271	VSS_360
AV39	VSS_NCTF_01	AV37	AY37	VSS_NCTF_03	
AV39	VSS_NCTF_02	AV37	B3	VSS_NCTF_04	



PLTRST_L Driving Circuit

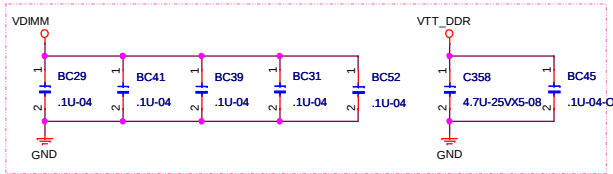
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ACA-ZIF-096-E02...LEAD-FREE(RoHS/HF).L0TES

20-800-005011 SUBASSY.STEEL...LGA 1155P...
W/BACK PLATE.ACA-ZIF-082-E23...LEAD-FREE(RoHS).L0TES

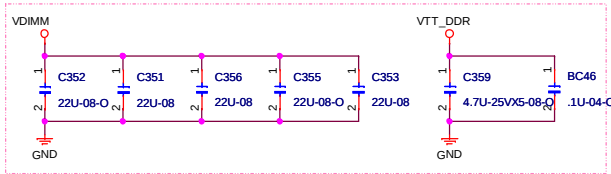


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CPU - GND, CPU_RST_L	
Size	Document Number
Custom	Q77H2-AD
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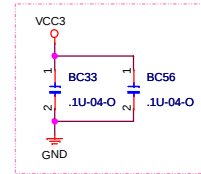
0.75V
MAX 1A



For CHAD1



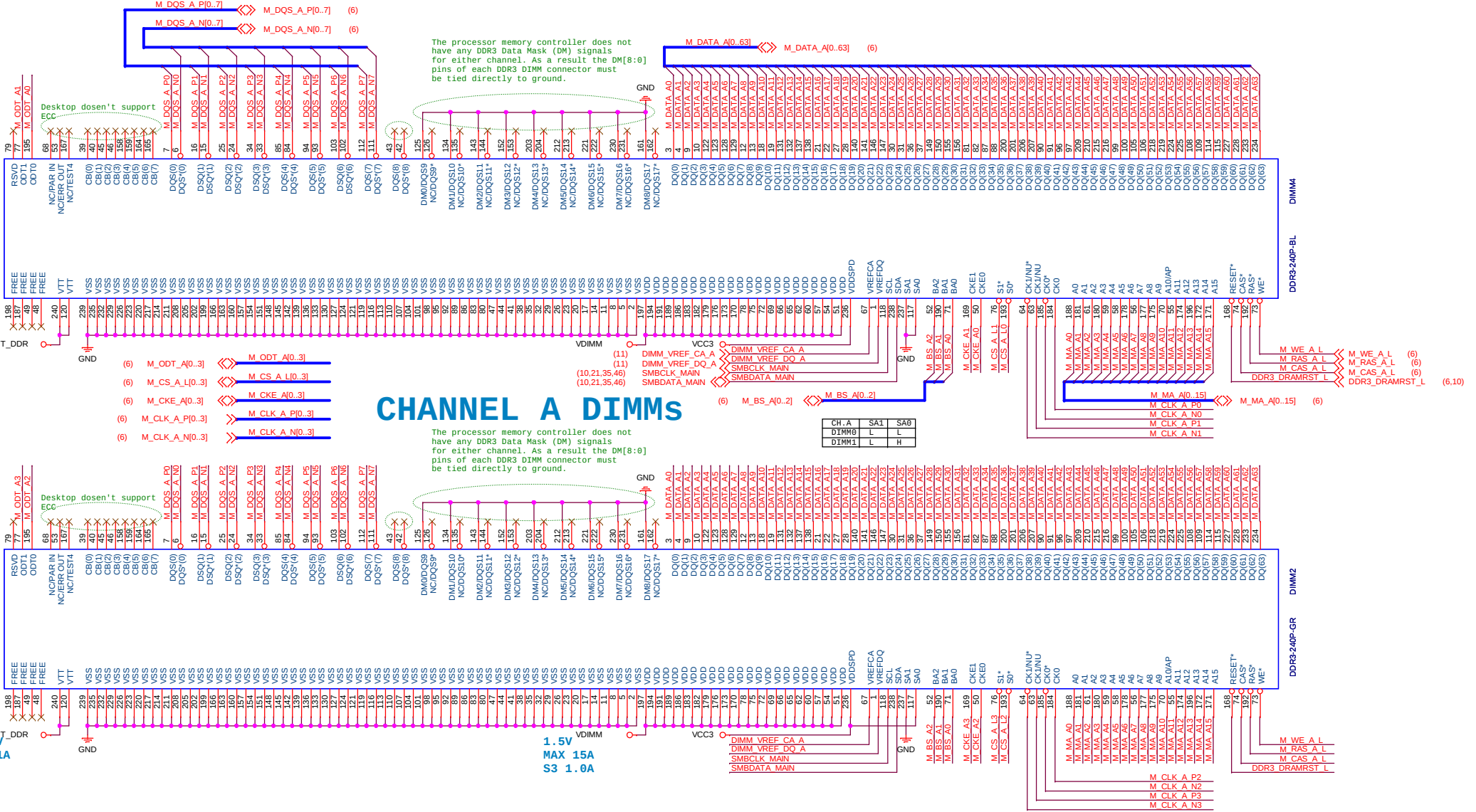
For CHAD2



PLACE BETWEEN CHA & CHB.
DO NOT PUNCH VIA.

CHANNEL A DIMMs

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

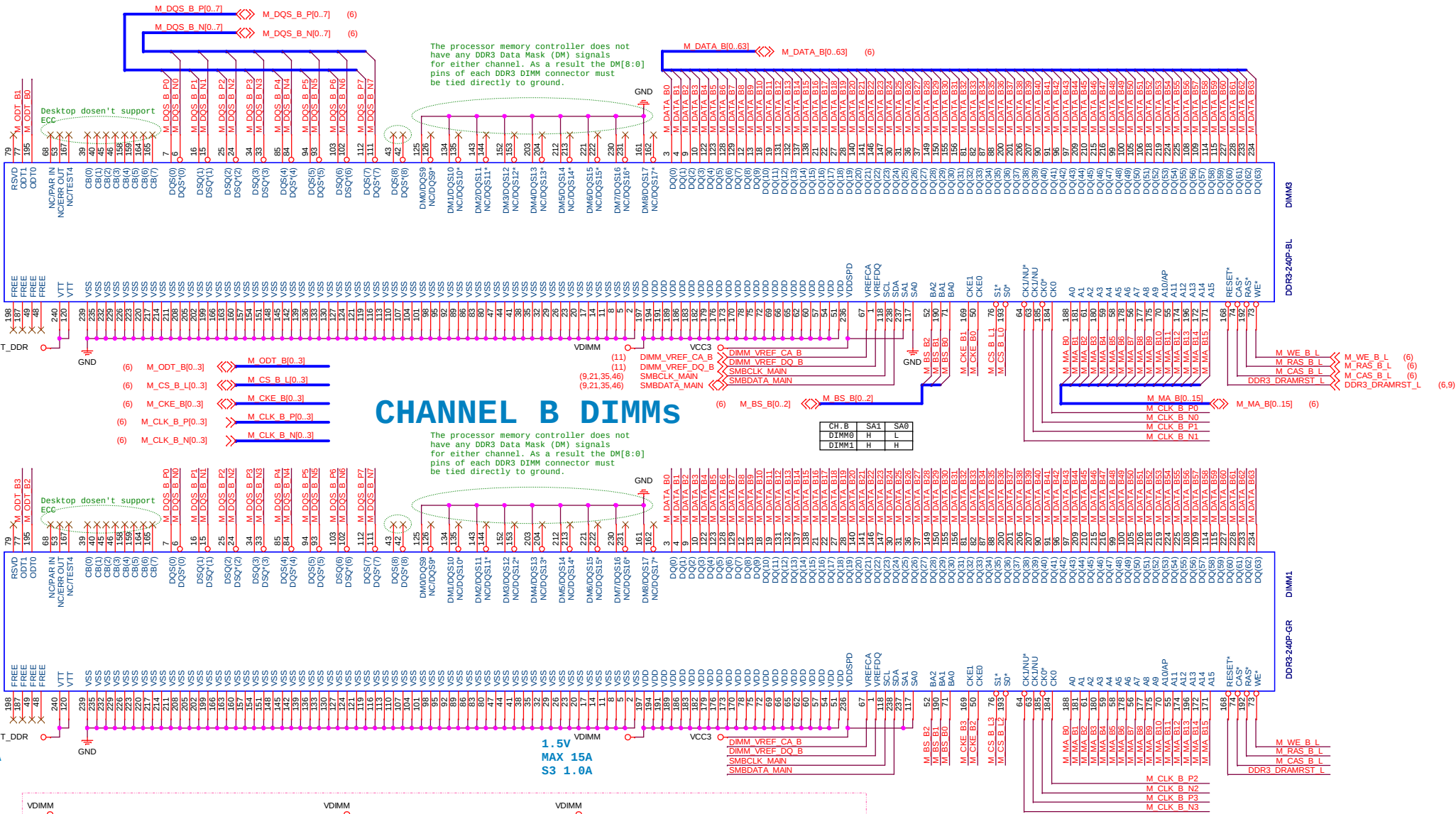


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0.75V
MAX 1A

CHANNEL B DIMMS

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



STITCHING CAPS FOR CMD, ADDR, CTL. BETWEEN CHBD1 & CHBD2

STITCHING CAPS FOR CMD, ADDR, CTL. BELOW CHBD3.

For CHBD1

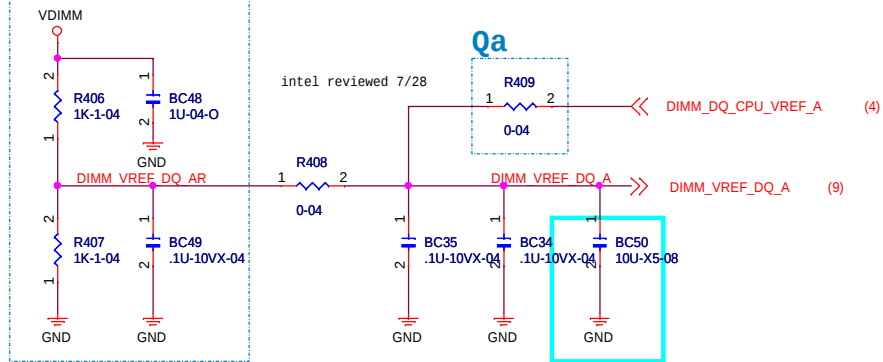
For CHBD2



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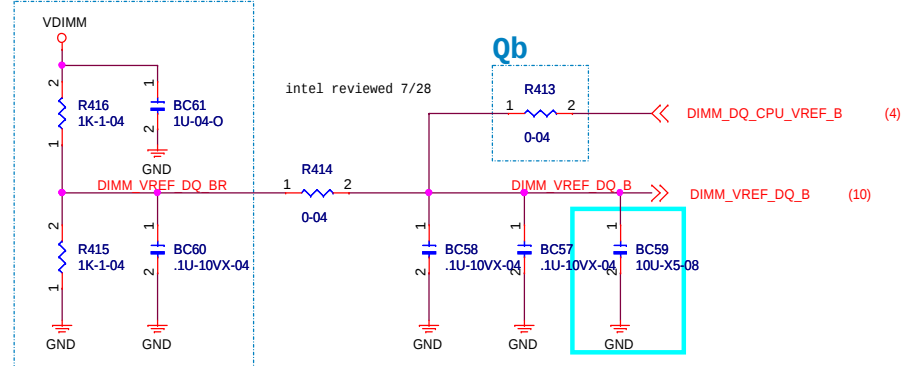
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Size	Document Number	Rev	
Custom	Q77H2-AD	1.0	
Date:	Tuesday, April 10, 2012	Sheet	10 of 49

Pa

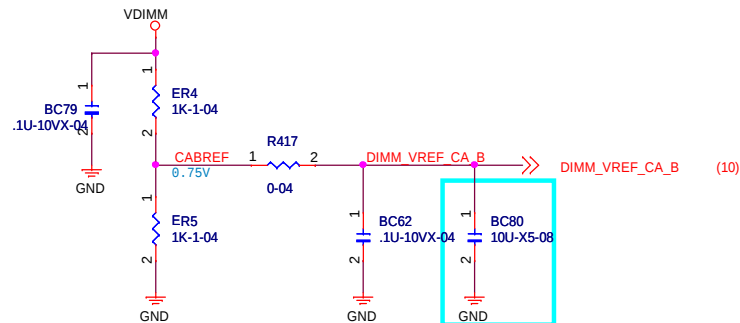
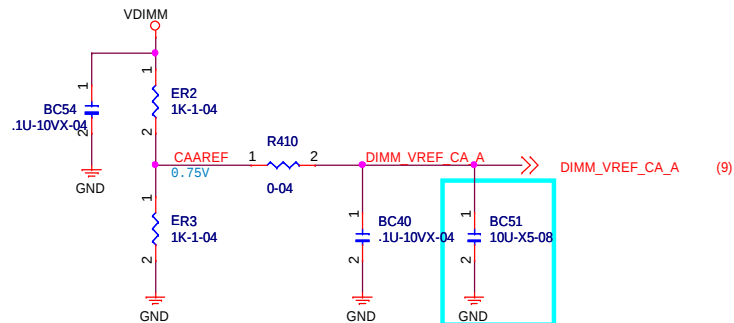


Layout Note:
All parts close to DDR3 Slots.

Pb



DIMM_VREF_DQ Control Circuit



DIMM_VREF_CA Circuit



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Title
DDR3 - VREF

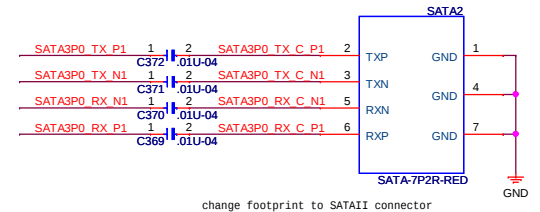
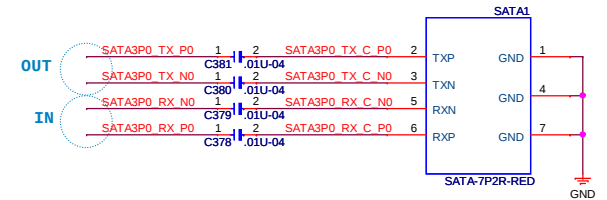
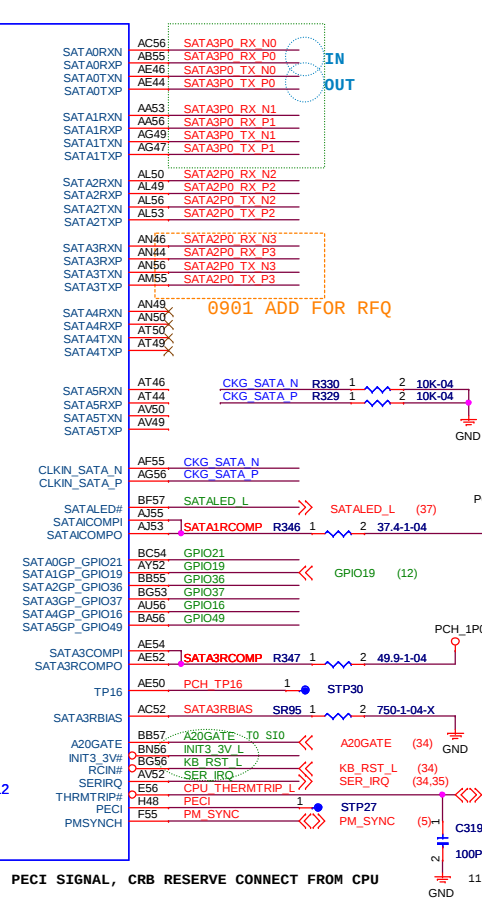
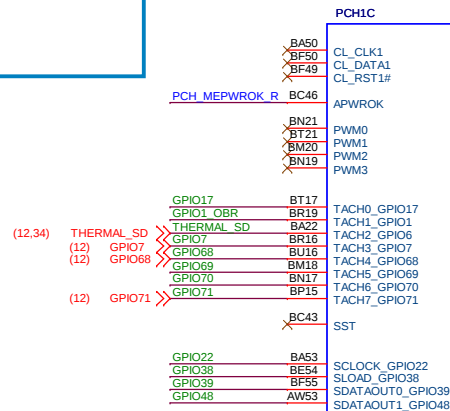
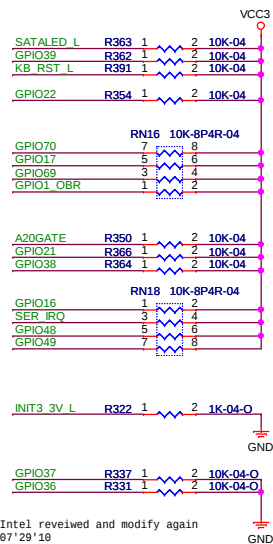
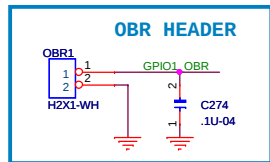
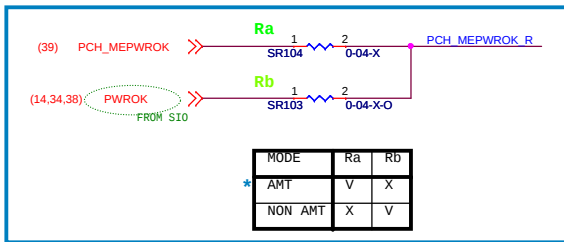
Size
Custom

Document Number
Q77H2-AD

Rev
1.0

Date: Tuesday, April 10, 2012

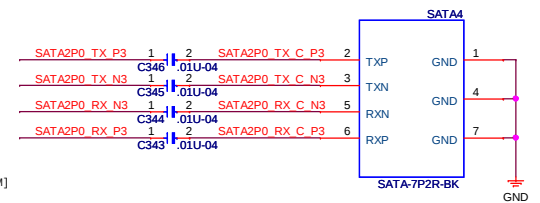
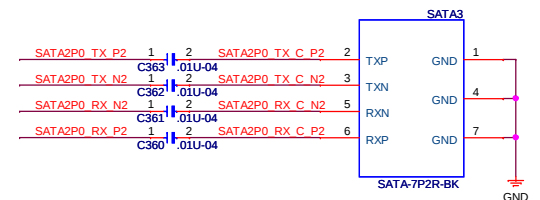
Sheet 11 of 49

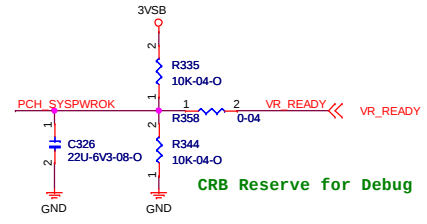
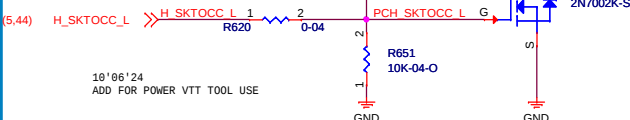
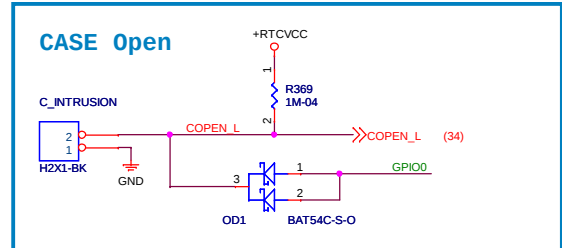
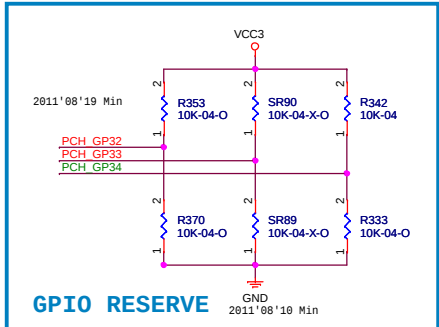
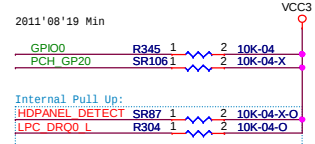
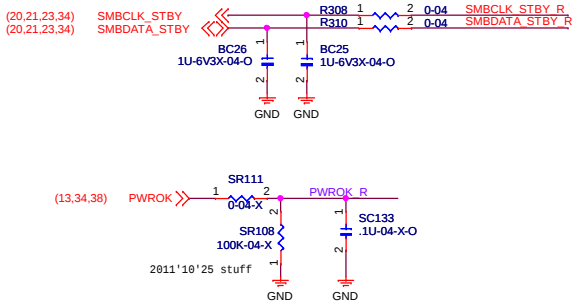
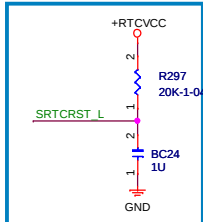
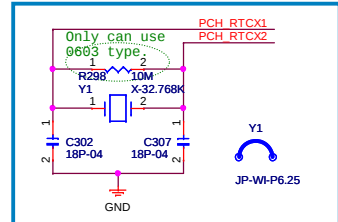
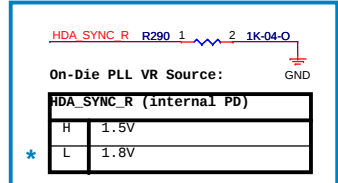
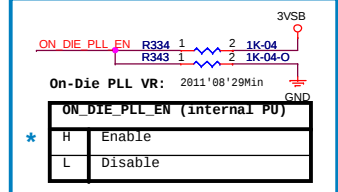
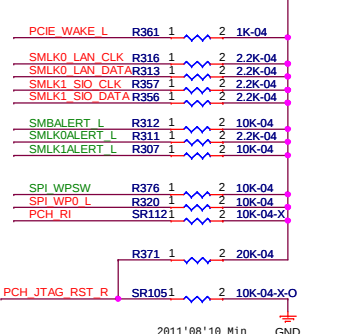
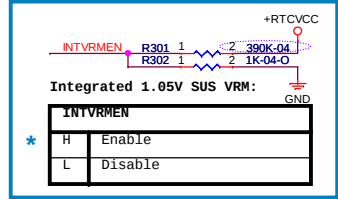
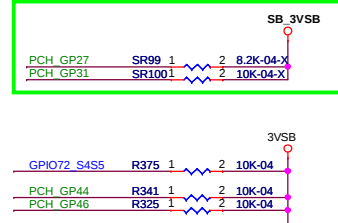
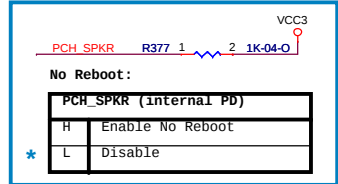
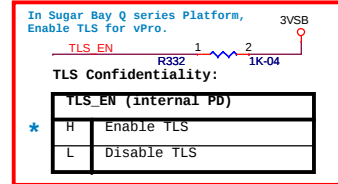
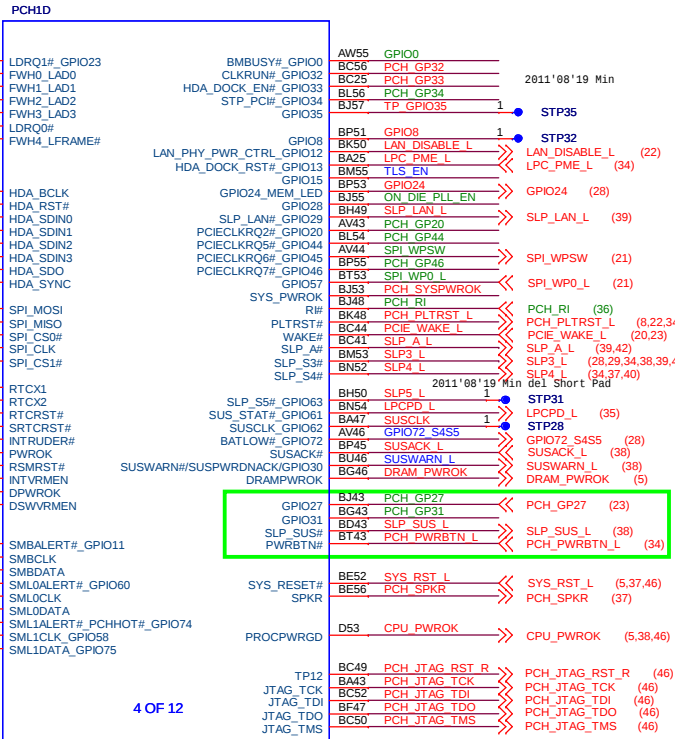
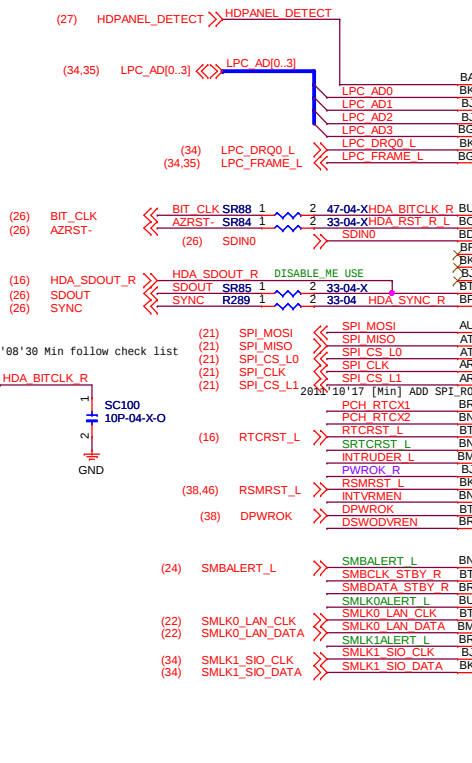


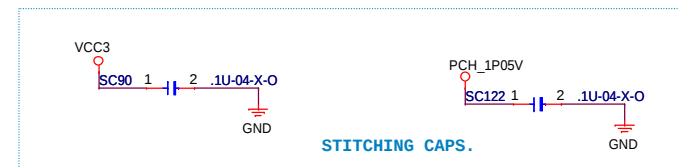
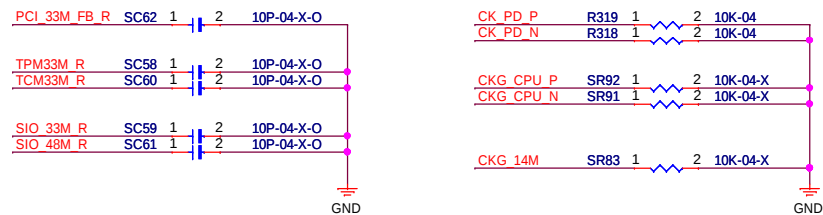
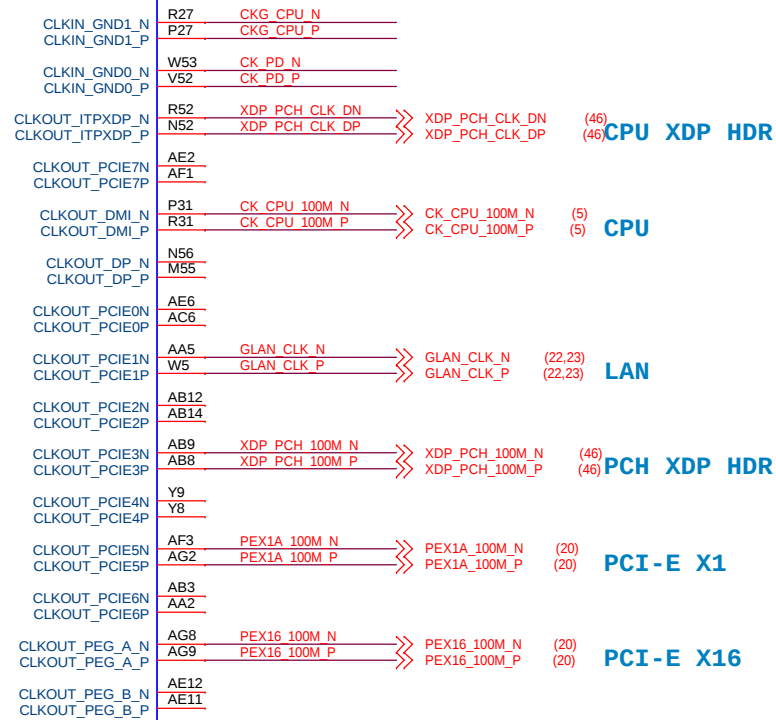
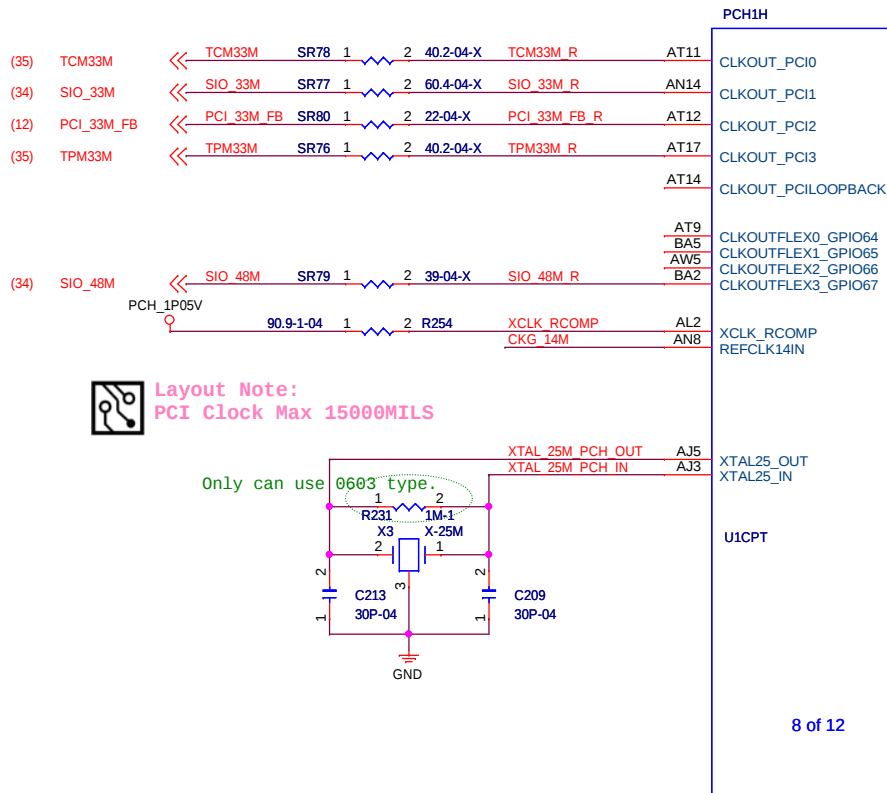
Layout Note:

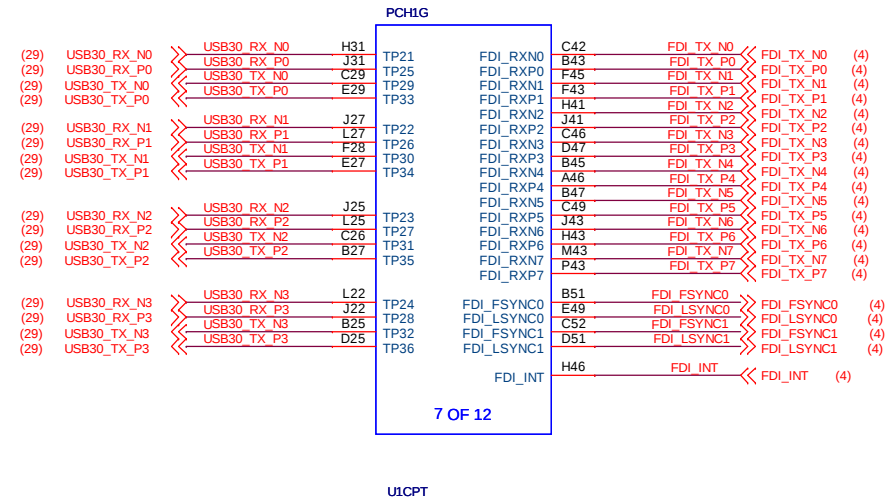
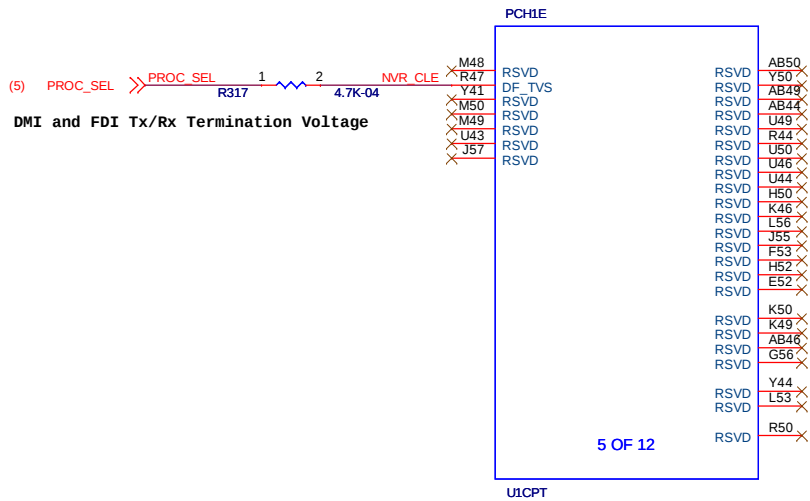
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%

SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

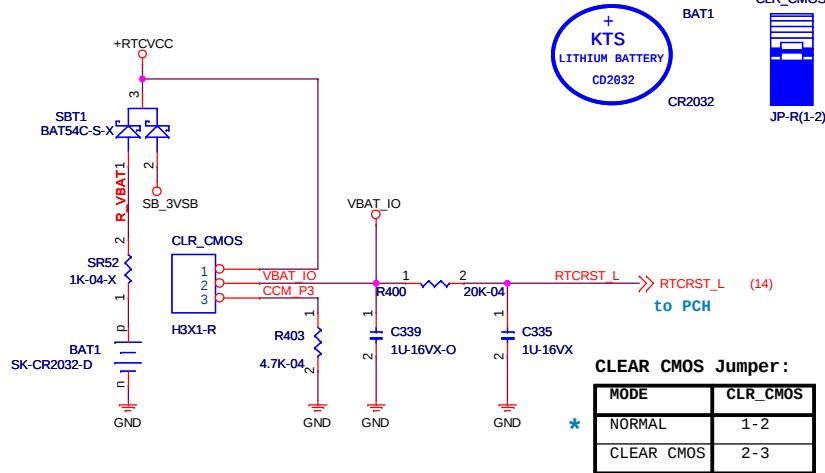




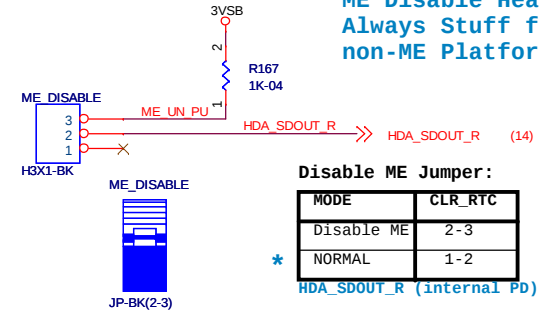




CLR_CMOS



**ME Disable Header,
Always Stuff for ME or
non-ME Platform.**



Elitegroup Computer Systems

Title **PCH - USB3.0/FDI, CLR_CMOS**

Size B Document Number **Q77H2-AD** Rev 1.0

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Port-B: DVII

Port-C: DP

Port-D: DP

[M 1007] PORTB CHANGE TO CONNECT TO DVI-I
PORT D CHANGE TO CONNECT TO DP

PCH1F

U1CPT

CRT_HSYNC
CRT_VSYNC

CRT_RED
CRT_GREEN
CRT_BLUE

CRT_IRTN
CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF

TP6
TP7
TP8
TP9

DDPC_CTRLCLK
DDPC_CTRLDATA

DDPD_CTRLCLK
DDPD_CTRLDATA

SDVO_CTRLCLK
SDVO_CTRLDATA

6 of 12

AR4 VGA_HSYNC R R274 2 1 33-04
AR2 VGA_VSYNC R R275 2 1 33-04

AN6 VGA RED
AN2 VGA GREEN
AM1 VGA BLUE

AM6
AW1
AW3
AT3
DACREFSET
SR81
1K-1-04-X

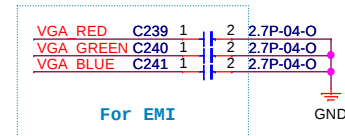
Y18 PCH TP6 1 STP21
Y17 PCH TP7 1 STP22
AB18 PCH TP8 1 STP17
AB17 PCH TP9 1 STP19

AL12
AL14
AL9
AL8
DDPD_CTRLCLK
DDPD_CTRLDATA
SR72 2 1 2.2K-04-X
SR71 2 1 2.2K-04-X

AL15
AL17
DDPB_CTRLCLK
DDPB_CTRLDATA

Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.
Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.
Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

[M 1007] PORTB CHANGE TO CONNECT TO DVI-I
PORT D CHANGE TO CONNECT TO DP



Elitegroup Computer Systems

Title
PCH - DISPLAY/VGA

Size Custom
Document Number
Q77H2-AD

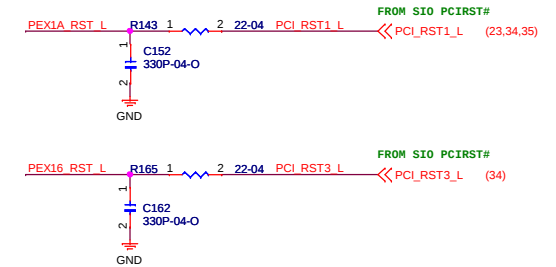
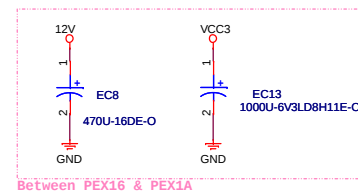
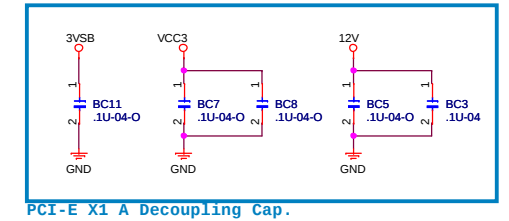
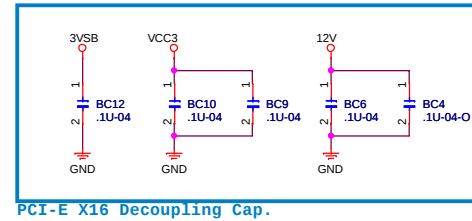
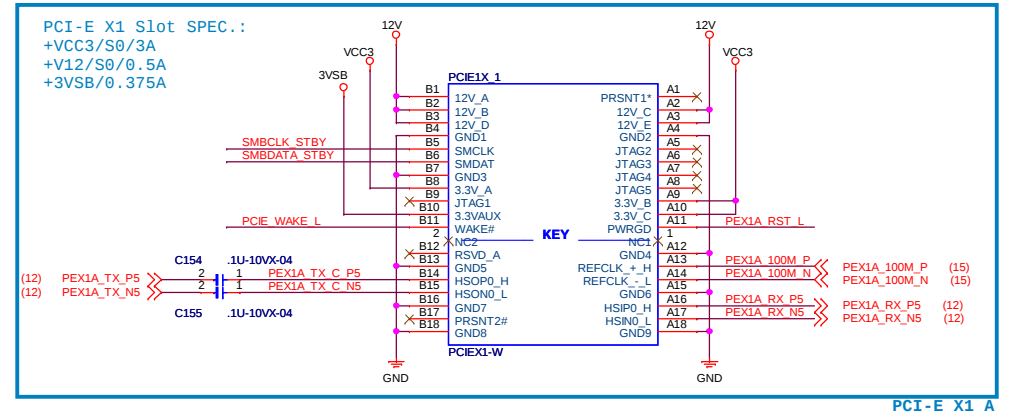
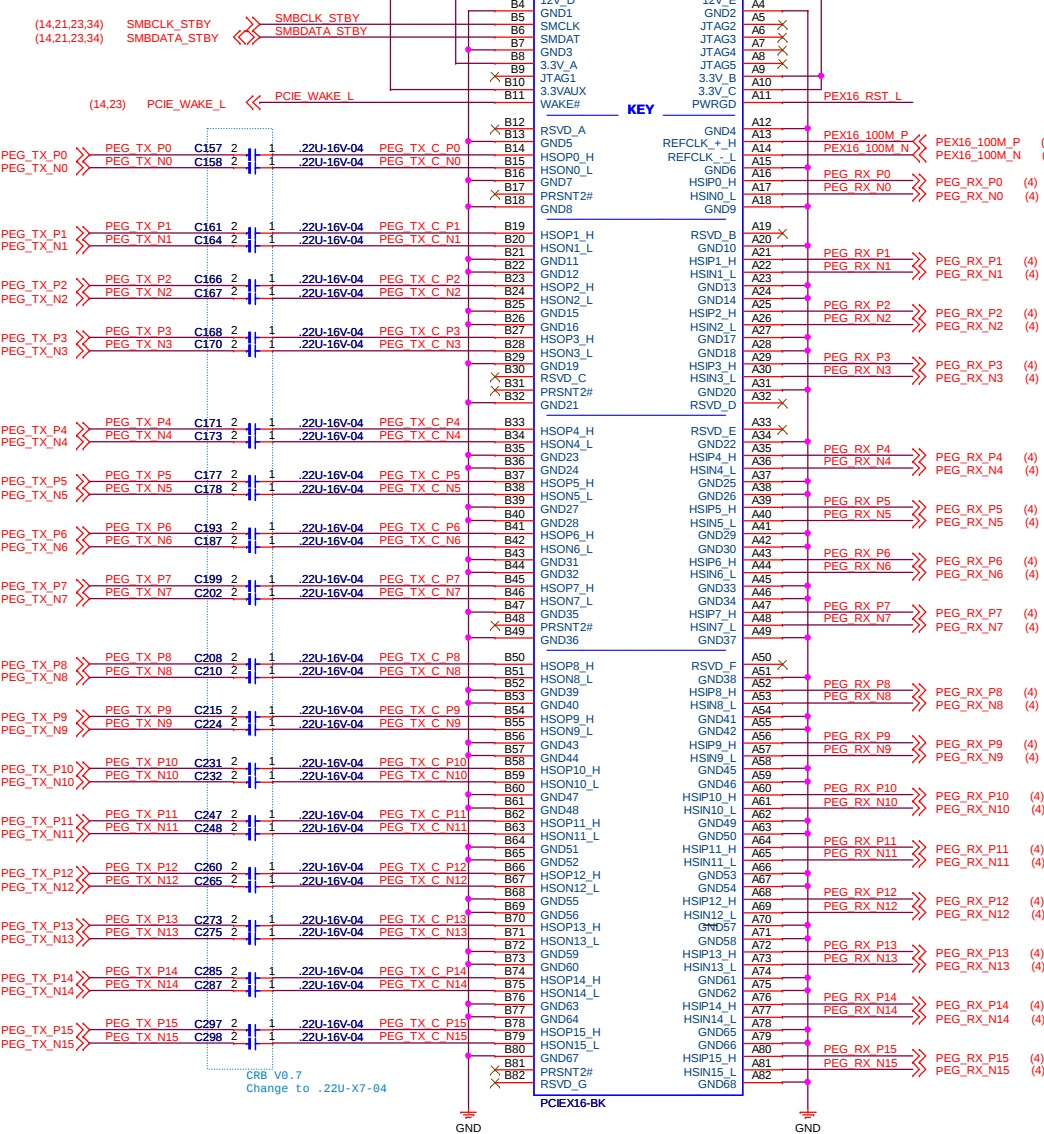
Rev
1.0.

Date: Tuesday, April 10, 2012 Sheet 17 of 49

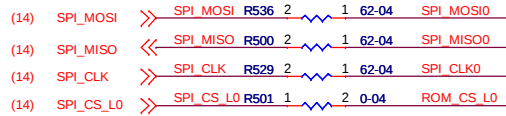
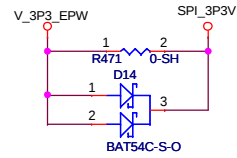


Sheet 18 of 49

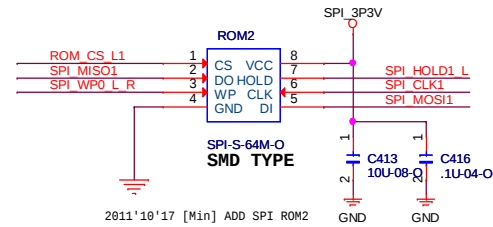
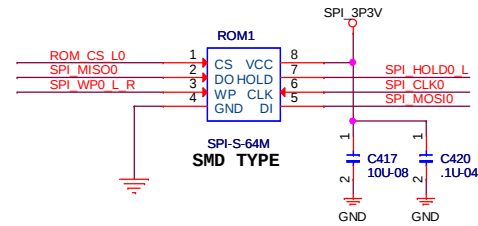
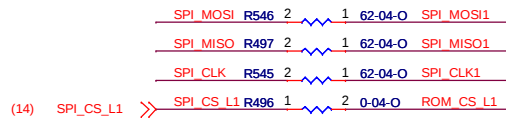
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



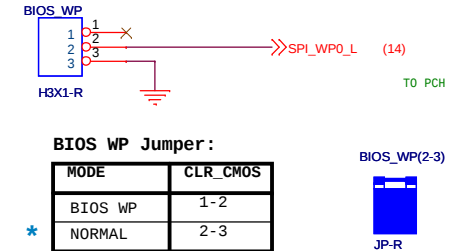
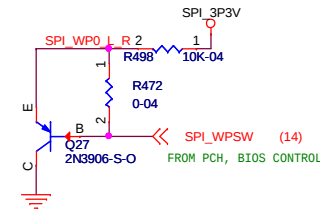
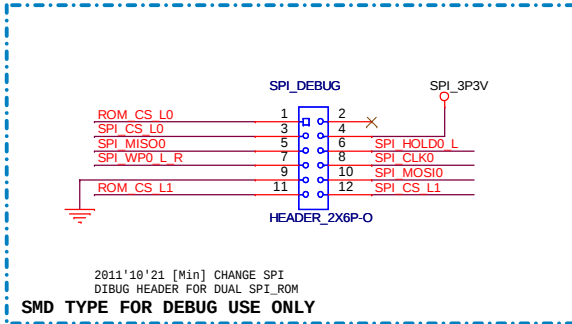
SPI ROM Circuit



11'12'06



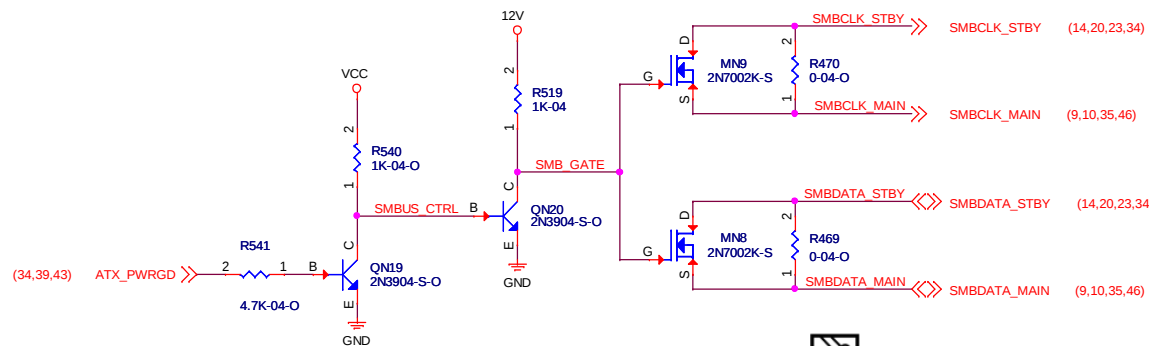
2011'10'17 [Min] ADD SPI ROM2



BIOS_WP Jumper:

MODE	CLR_CMOS
BIOS_WP	1-2
NORMAL	2-3

SMBUS Logic Circuit

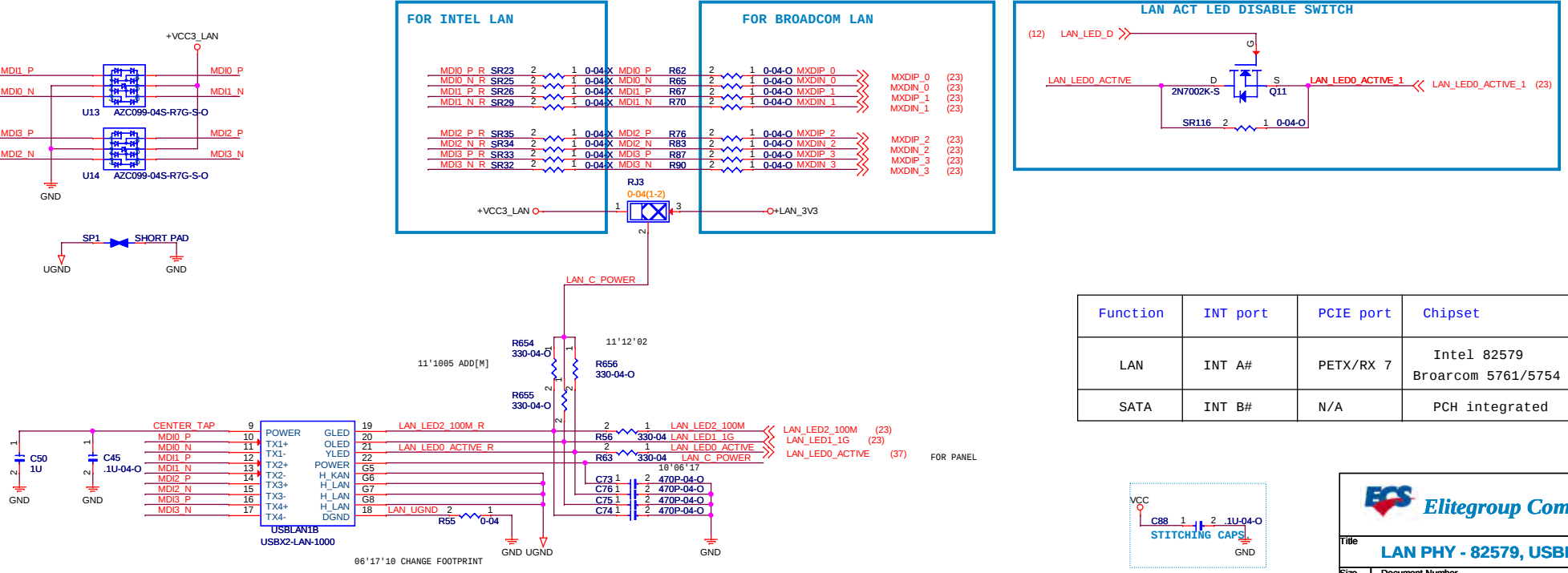
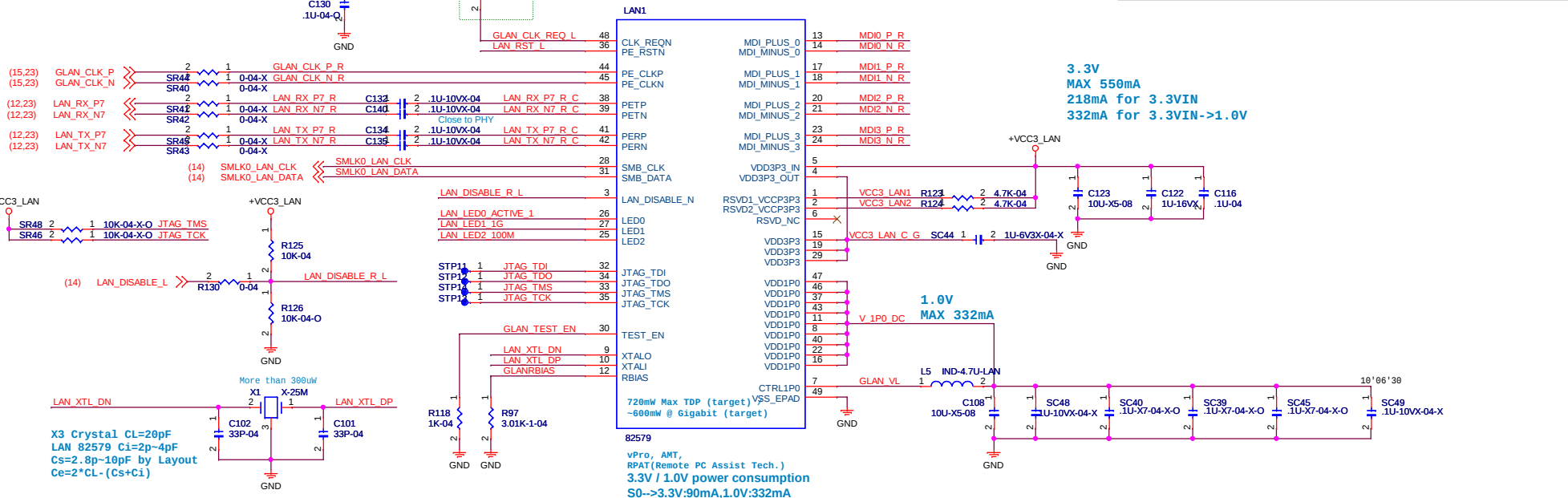


Layout Note:
SMBUS Trace Max 21500MILS



Elitegroup Computer Systems

Title SPI ROM, SMBUS		
Size Custom	Document Number Q77H2-AD	Rev 1.0.
Date: Tuesday, April 10, 2012	Sheet 21	of 49



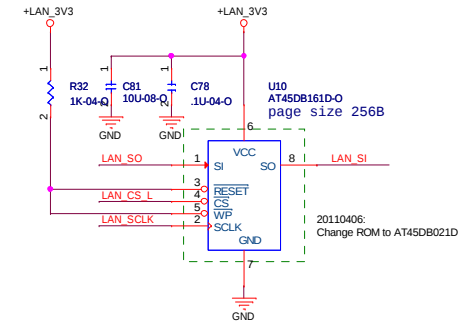
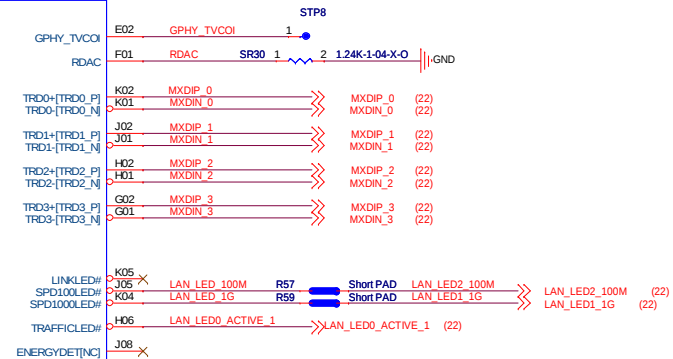
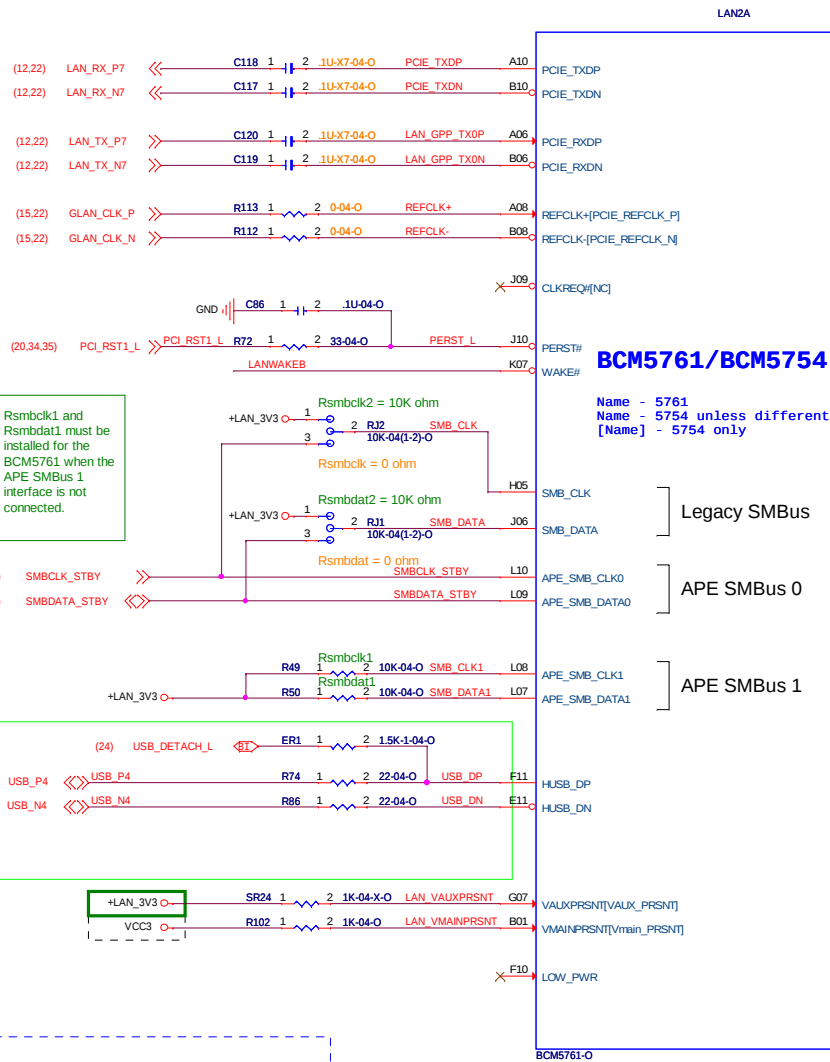
Function	INT port	PCIE port	Chipset
LAN	INT A#	PETX/RX 7	Intel 82579 Broarcom 5761/5754
SATA	INT B#	N/A	PCH integrated

**Elitegroup Computer Systems**

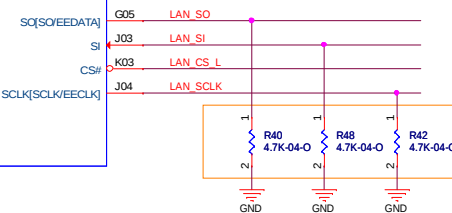
Title**LAN PHY - 82579, USBLAN**

Size CustomDocument Number**Q77H2-AD**Rev**1.0**

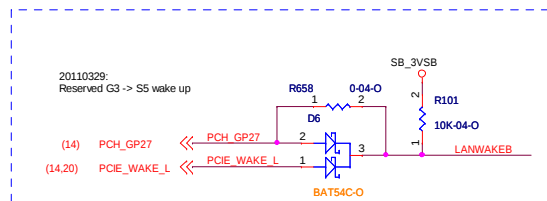
Date**Tuesday, April 10, 2012**Sheet**22** of **49**



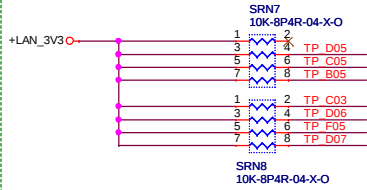
Flash device shown is for the BCM5761 only. Refer to the BCM5754 data sheet for supported flash devices.



These resistors must be installed with the BCM5754 to configure flash auto-sense.



These resistors must be installed with the BCM5761 only.



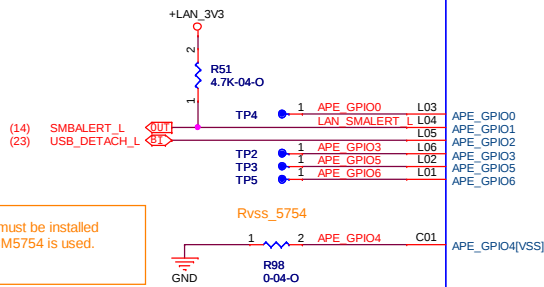
Ruart_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8_pd must be installed with the BCM5761 only.

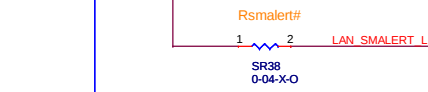
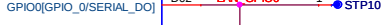
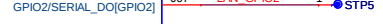
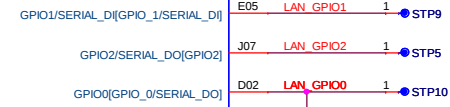
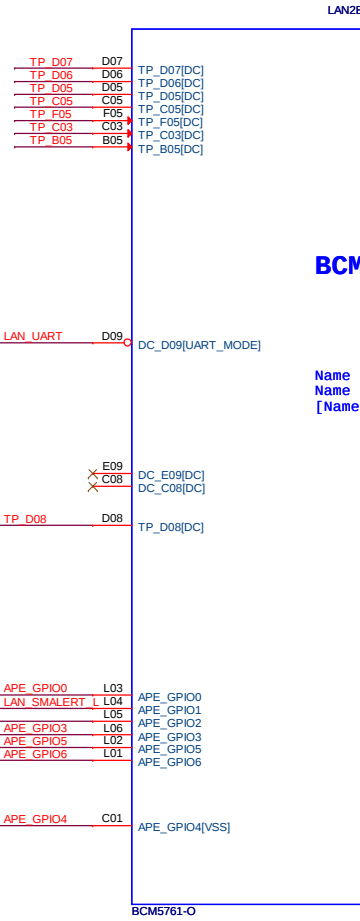


Rvss_5754 must be installed when the BCM5754 is used.

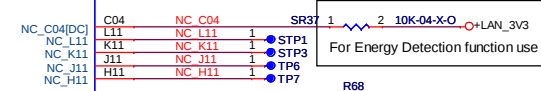


BCM5761/BCM5754

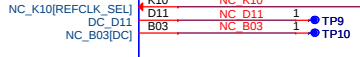
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



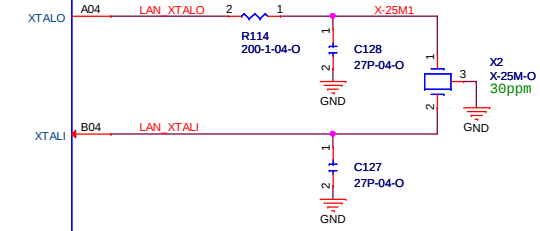
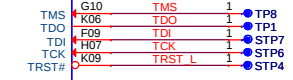
Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.



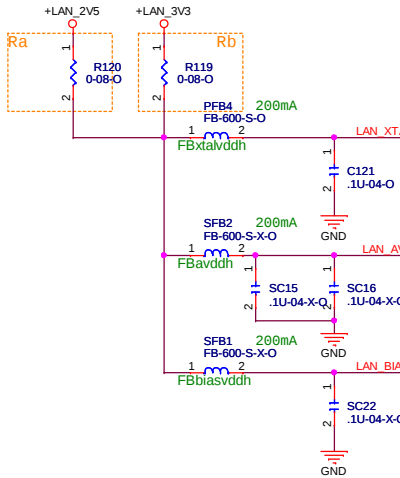
For Energy Detection function use only for 5761E use



Rrefcksel must not be installed with the BCM5761, but may be installed with the BCM5754

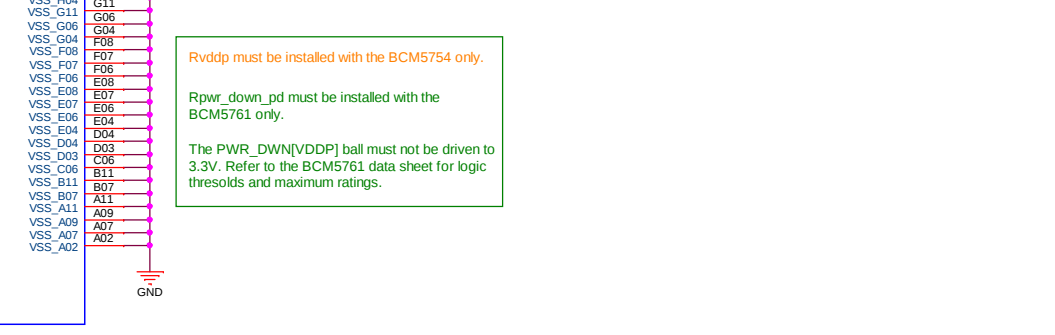
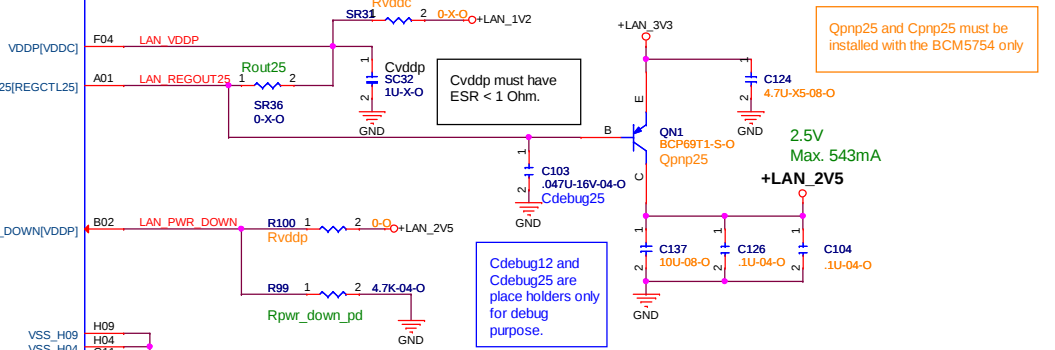
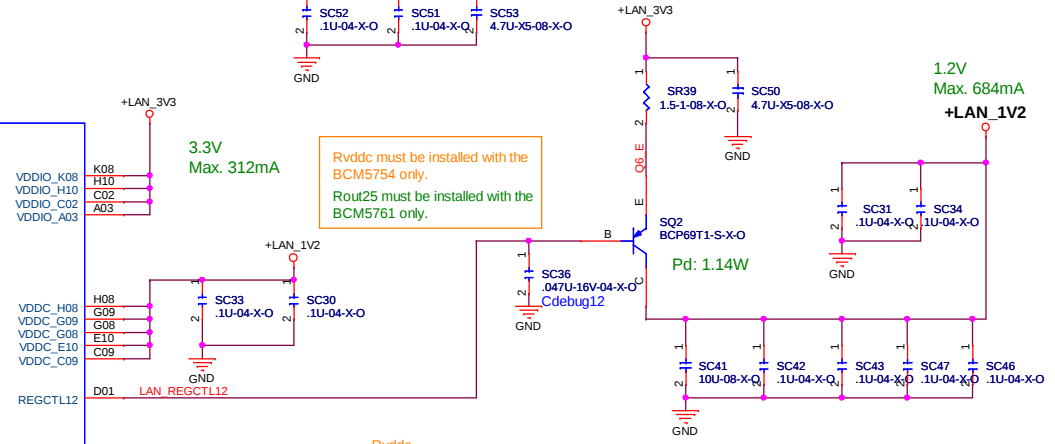


	5754	5761
Ra	V	X
Rb	X	V



BCM5761/BCM5754

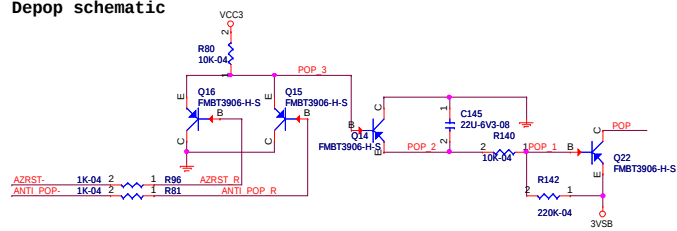
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



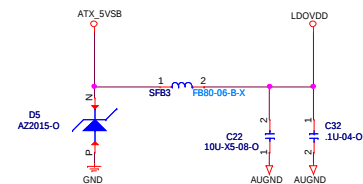
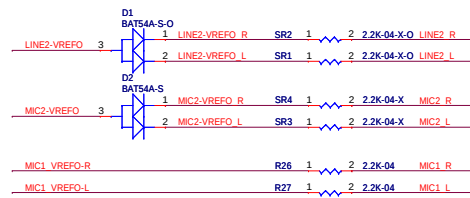
If the BCM5761 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf may be uninstalled.

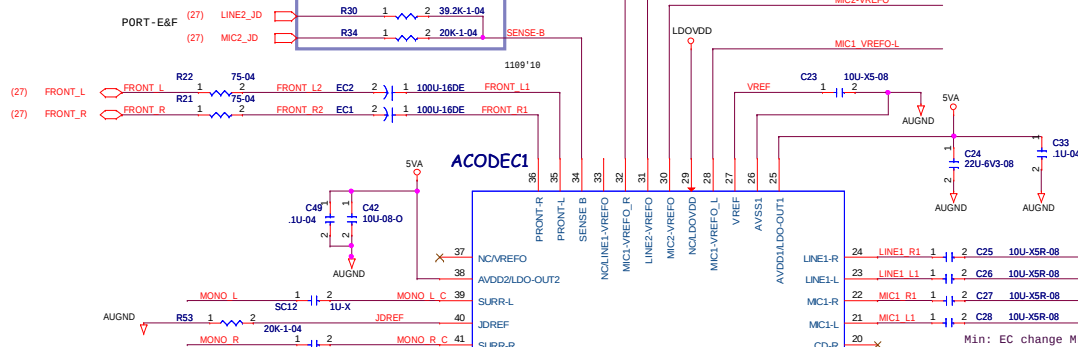
Depop schematic



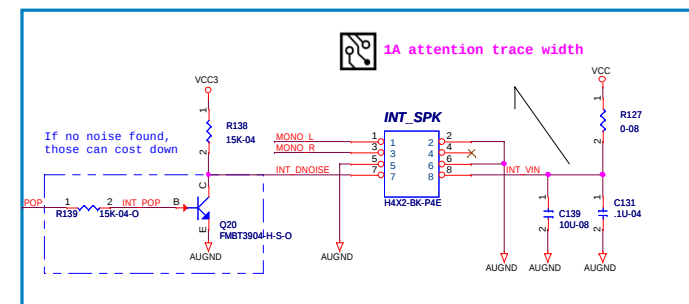
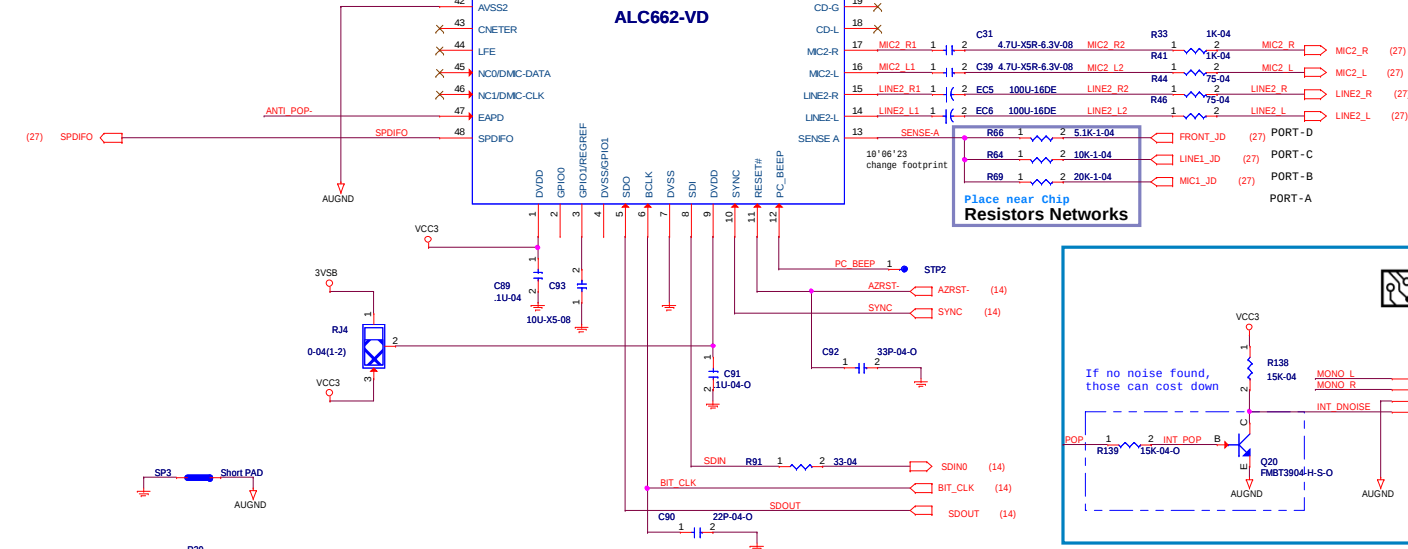
MIC Bias



Resistors Networks

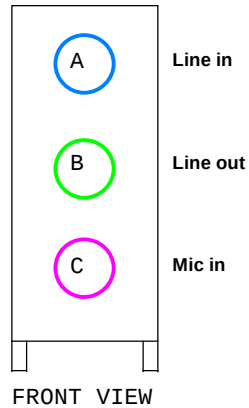
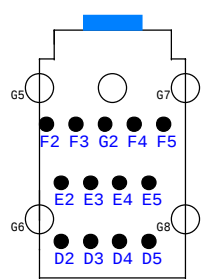
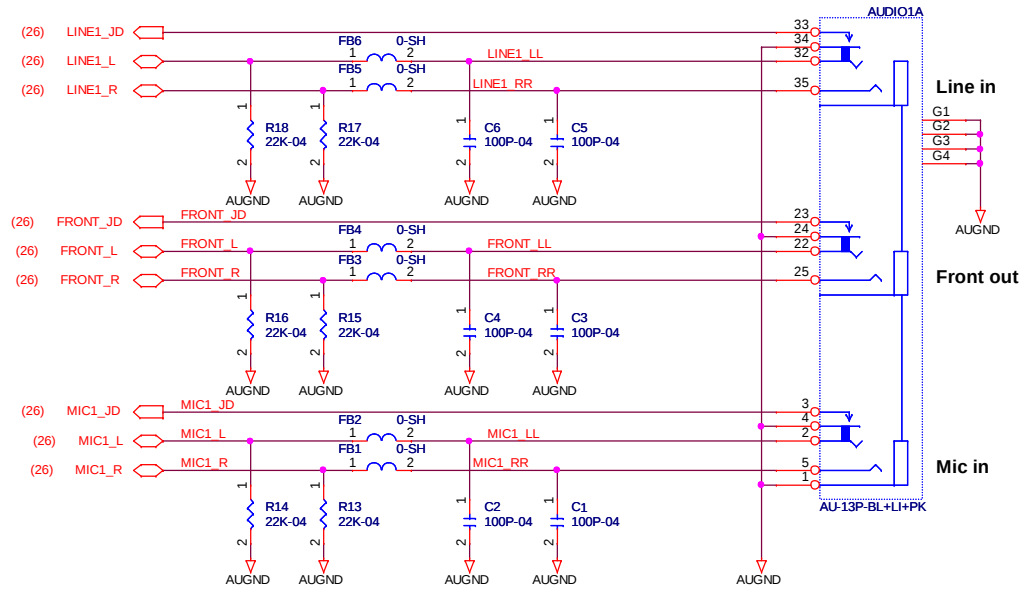


ALC662-VD

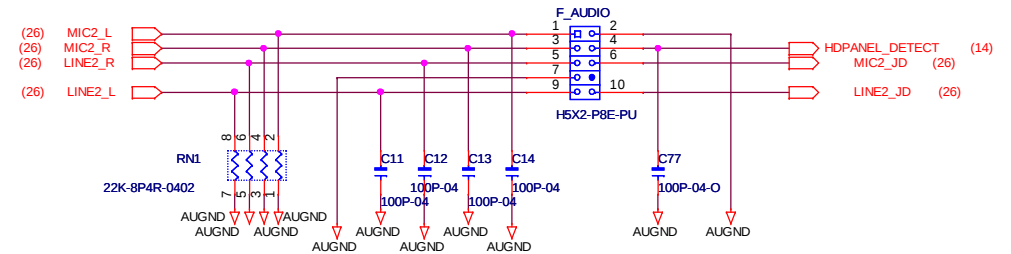


**"INTERNAL SPEAKER"
FOR COMMERCIAL AND AIO SERIES USE**

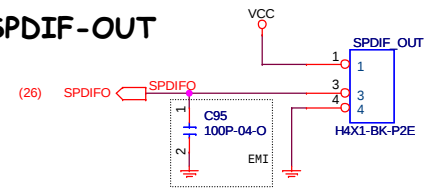
REAR-AUDIO



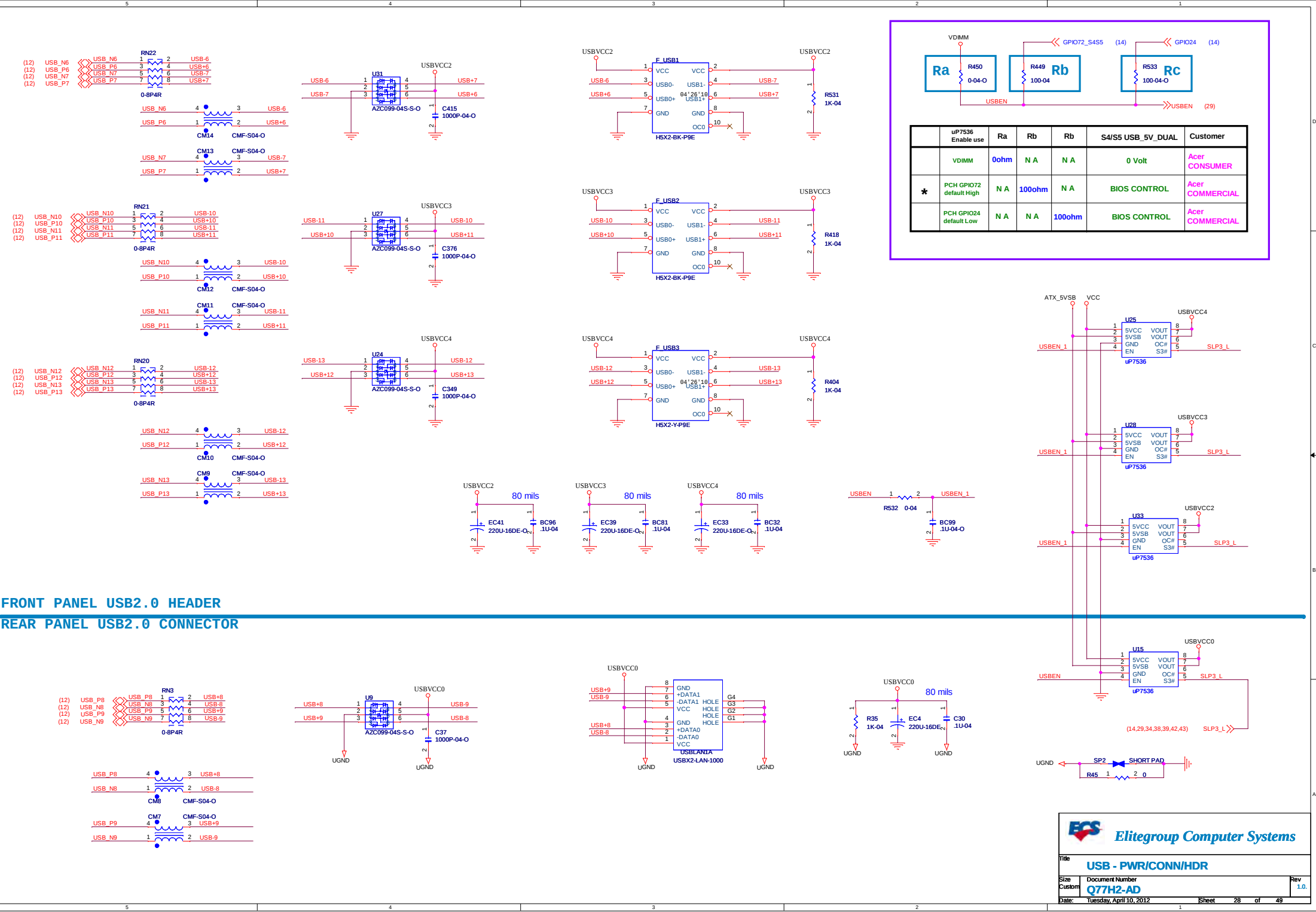
FRONT-AUDIO

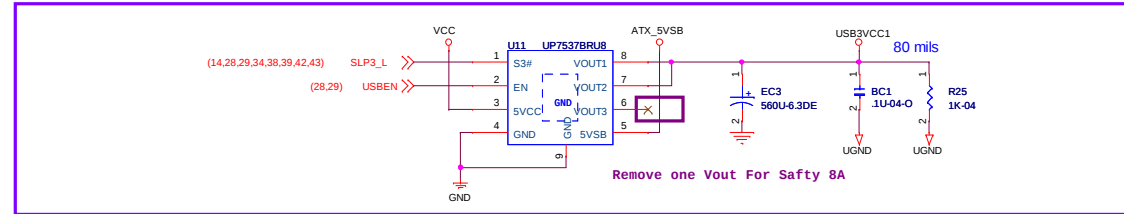
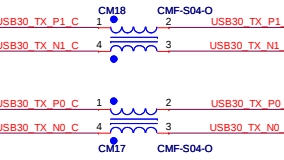
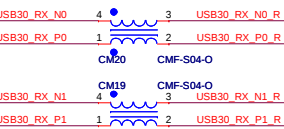
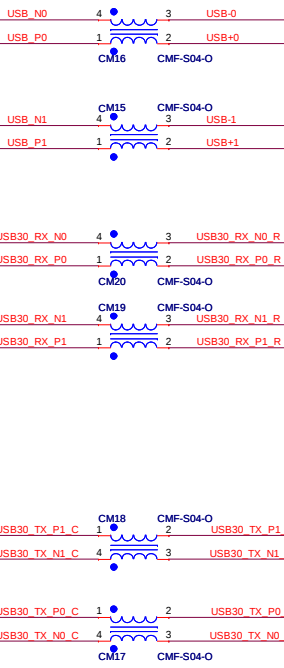
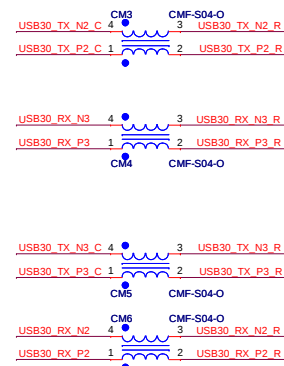
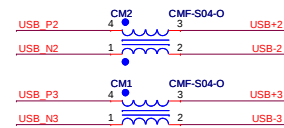
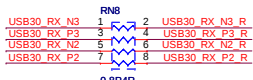
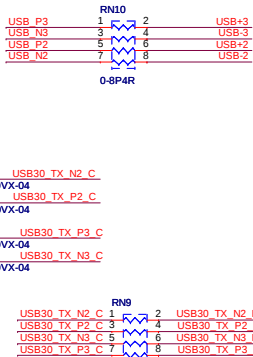
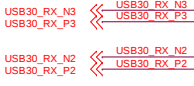
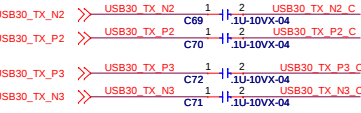


SPDIF-OUT

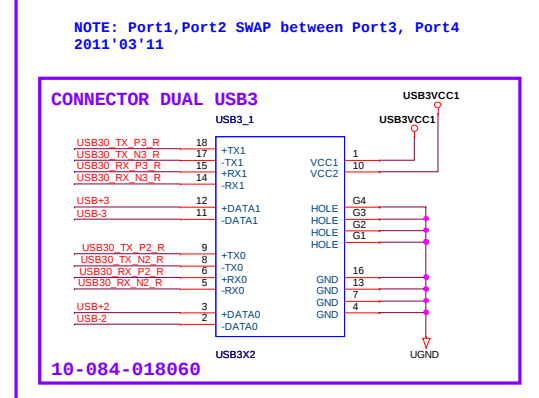
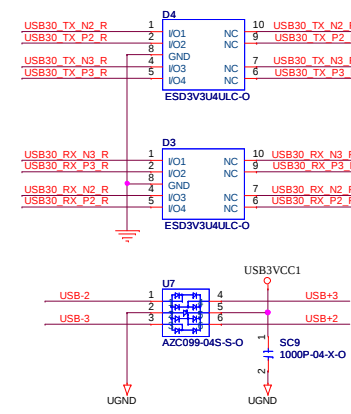


AUDIO ALC662 Connector (PANEL)	
Title	Rev 1.0
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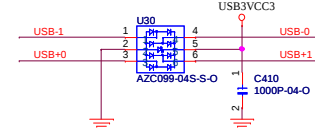
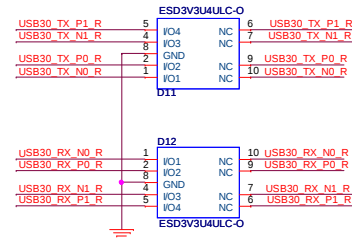
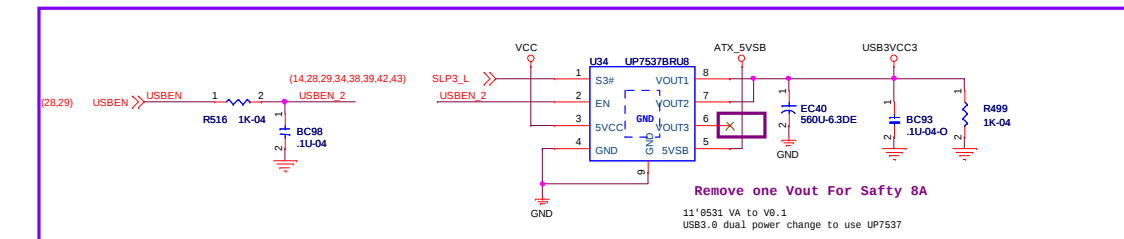
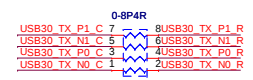
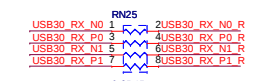
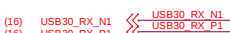
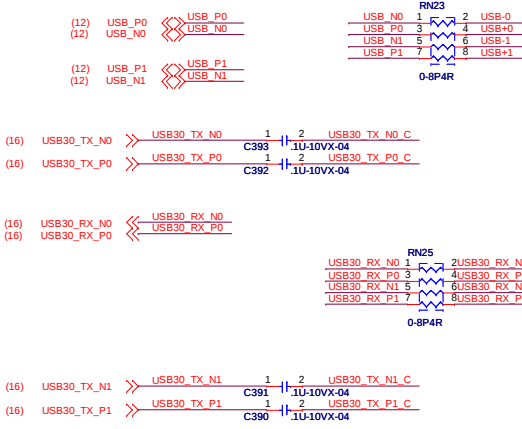


USB3 ESD COMPONENTS

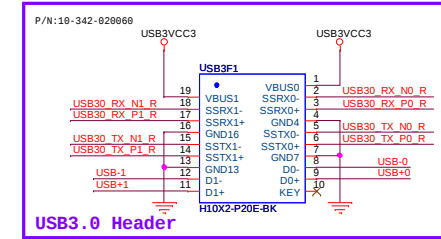


REAR PANEL USB3.0 CONNECTOR

FRONT PANEL USB3.0 HEADER



USB3 ESD COMPONENTS

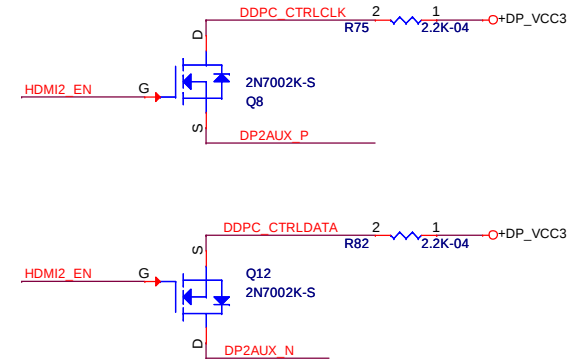
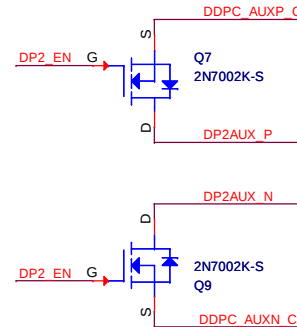
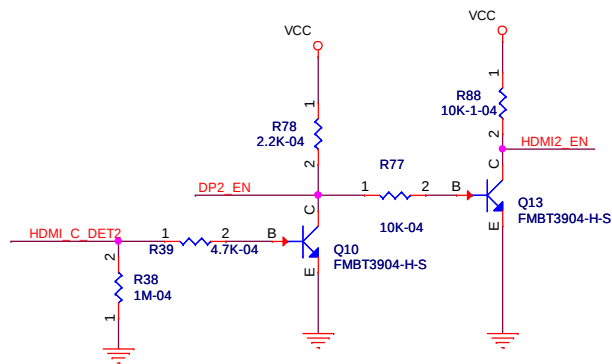
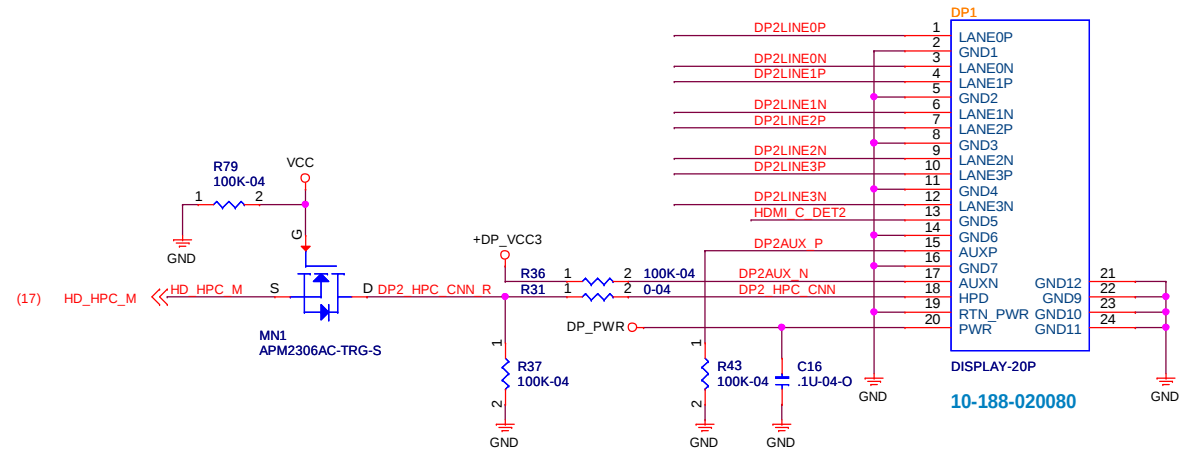


(17) DDPC_CTRLDATA >> DDPC_CTRLDATA
(17) DDPC_CTRLCLK >> DDPC_CTRLCLK

(17) DDPC_AUXP >> DDPC_AUXP C44 >> 1U-10VX-04 DDPC_AUXP C
(17) DDPC_AUXN >> DDPC_AUXN C41 >> 1U-10VX-04 DDPC_AUXN C

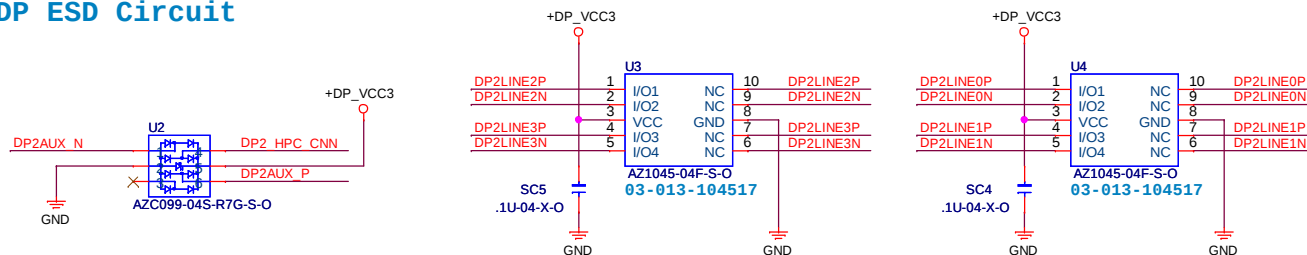
(17) DDPC_0P >> DDPC_0P C53 >> 1U-10VX-04 DP2LINE0P C 8 7 DP2LINE0P
(17) DDPC_0N >> DDPC_0N C54 >> 1U-10VX-04 DP2LINE0N C 6 5 DP2LINE0N
(17) DDPC_1P >> DDPC_1P C55 >> 1U-10VX-04 DP2LINE1P C 4 3 DP2LINE1P
(17) DDPC_1N >> DDPC_1N C56 >> 1U-10VX-04 DP2LINE1N C 2 1 DP2LINE1N

(17) DDPC_2P >> DDPC_2P C57 >> 1U-10VX-04 DP2LINE2P C 8 7 DP2LINE2P
(17) DDPC_2N >> DDPC_2N C58 >> 1U-10VX-04 DP2LINE2N C 6 5 DP2LINE2N
(17) DDPC_3P >> DDPC_3P C59 >> 1U-10VX-04 DP2LINE3P C 4 3 DP2LINE3P
(17) DDPC_3N >> DDPC_3N C60 >> 1U-10VX-04 DP2LINE3N C 2 1 DP2LINE3N



SUPPORT DP TO HDMI/DVI DONGLE

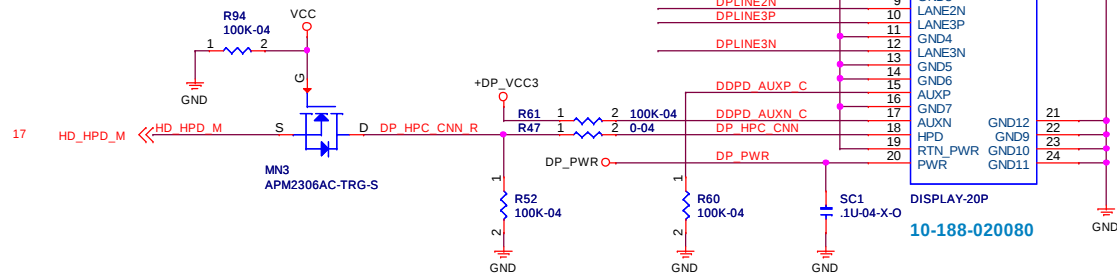
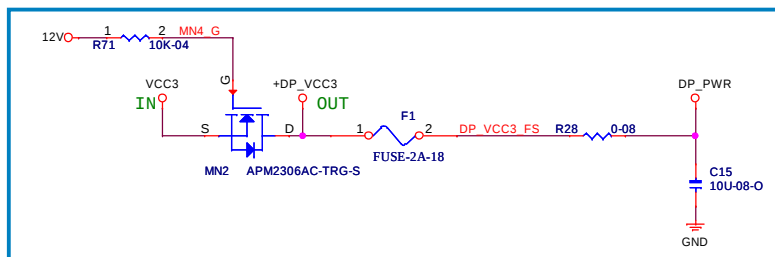
DP ESD Circuit



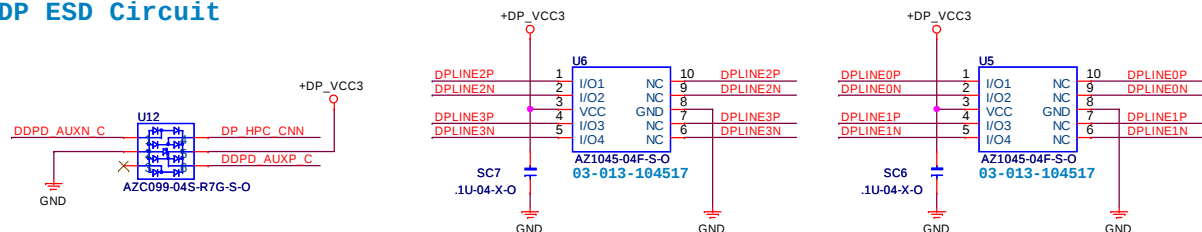
DDPD_AUXP >> DDPD_AUXP C80 >> 1U-10VX-04 DDPD_AUXP C
DDPD_AUXN >> DDPD_AUXN C79 >> 1U-10VX-04 DDPD_AUXN C

DDPD_0P >> DDPD_0P C61 >> 1U-10VX-04 DPLINE0P C 8 7 DPLINE0P
DDPD_0N >> DDPD_0N C62 >> 1U-10VX-04 DPLINE0N C 6 5 DPLINE0N
DDPD_1P >> DDPD_1P C63 >> 1U-10VX-04 DPLINE1P C 4 3 DPLINE1P
DDPD_1N >> DDPD_1N C64 >> 1U-10VX-04 DPLINE1N C 2 1 DPLINE1N
RN6

DDPD_2P >> DDPD_2P C65 >> 1U-10VX-04 DPLINE2P C 8 7 DPLINE2P
DDPD_2N >> DDPD_2N C66 >> 1U-10VX-04 DPLINE2N C 6 5 DPLINE2N
DDPD_3P >> DDPD_3P C67 >> 1U-10VX-04 DPLINE3P C 4 3 DPLINE3P
DDPD_3N >> DDPD_3N C68 >> 1U-10VX-04 DPLINE3N C 2 1 DPLINE3N
RN7



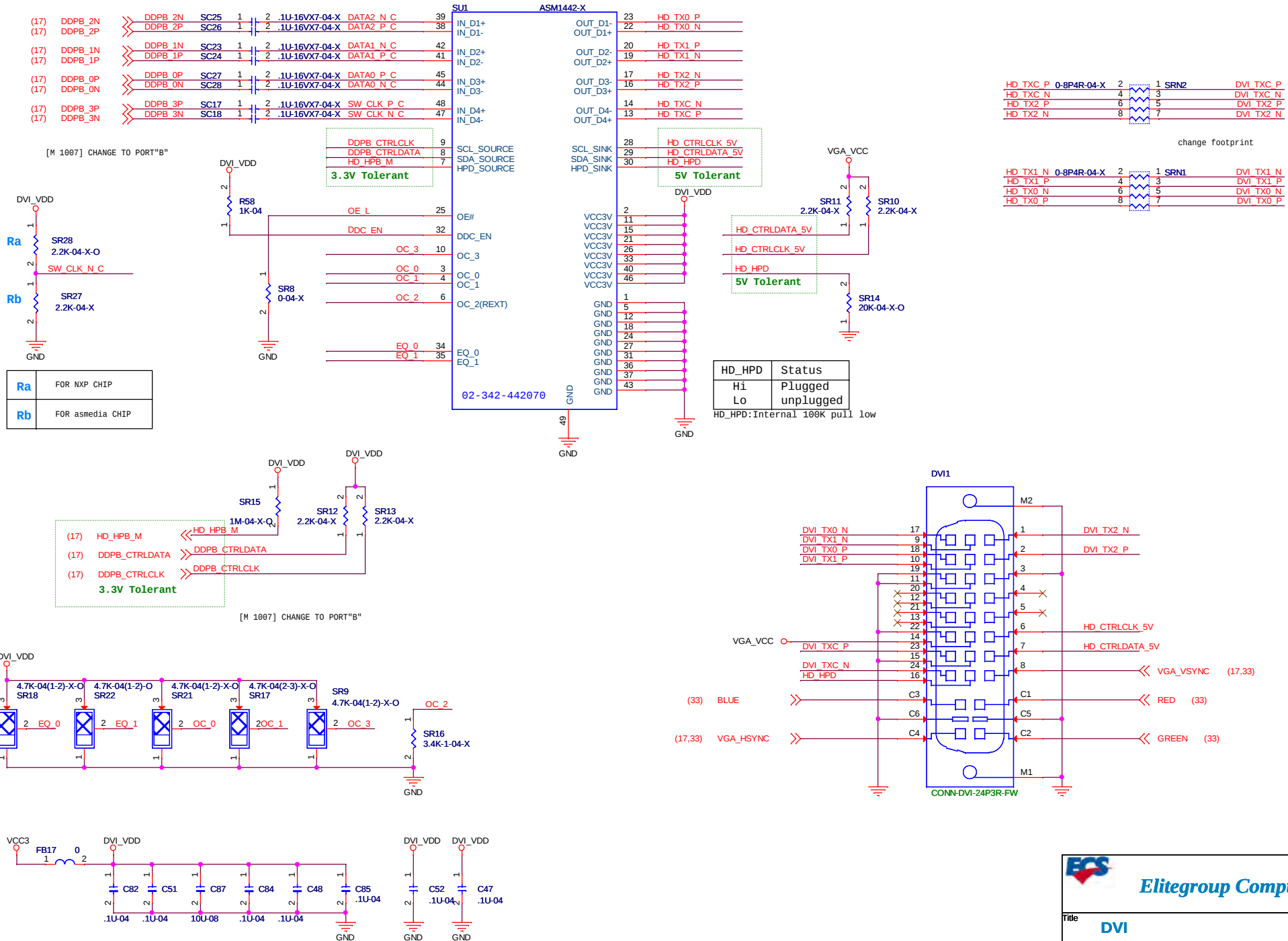
DP ESD Circuit

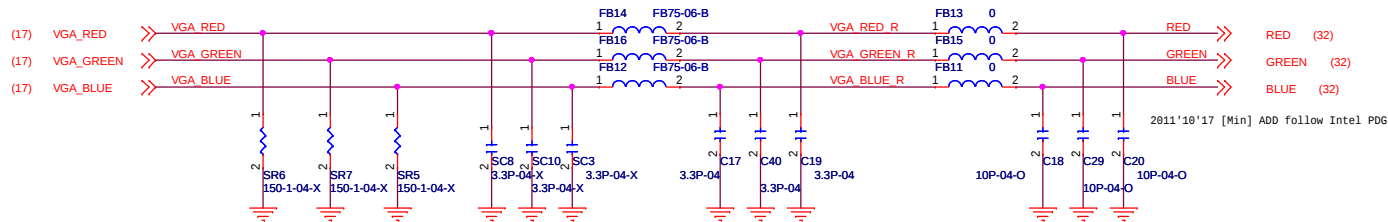


DISPLAY PORT2

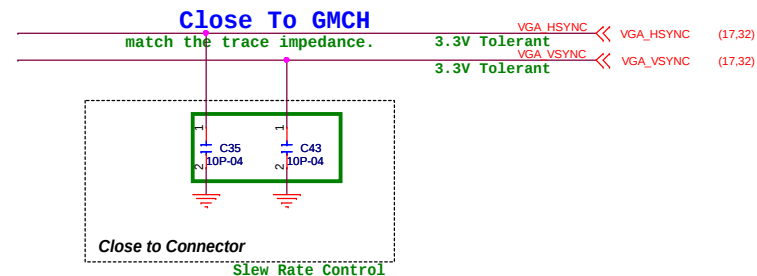
Size Custom Document Number Q77H2-AD Rev 1.0
Date: Tuesday, April 10, 2012 Sheet 31 of 49

Level Shifter



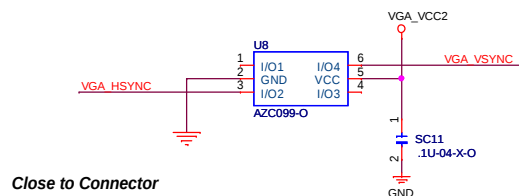


Close to Connector

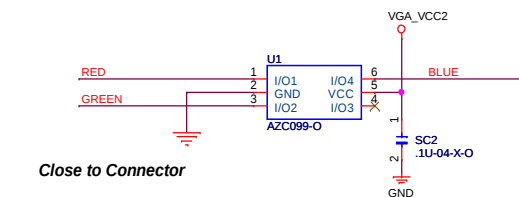


Close to Connector

Slew Rate Control

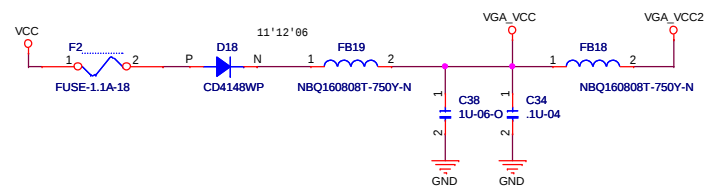


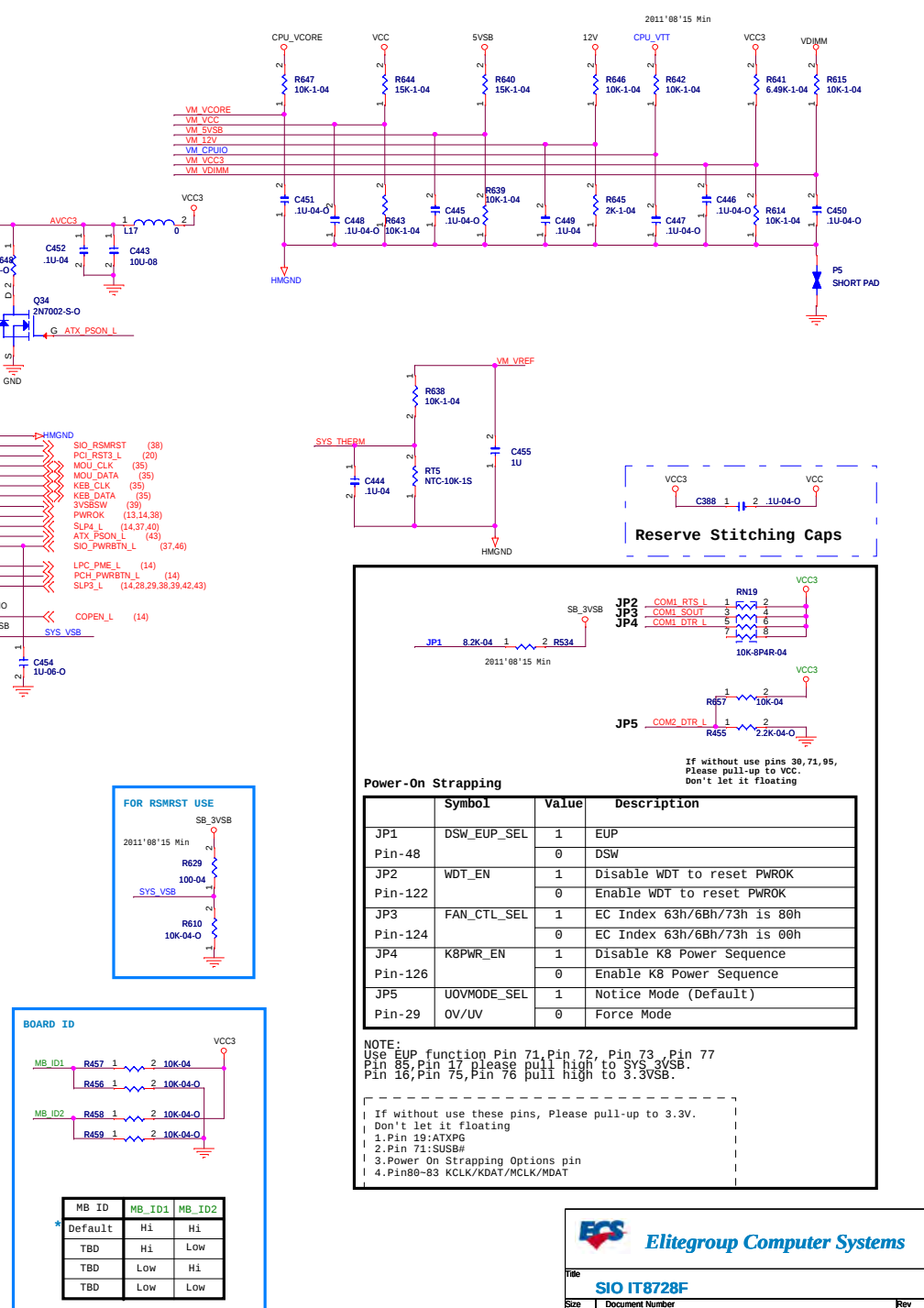
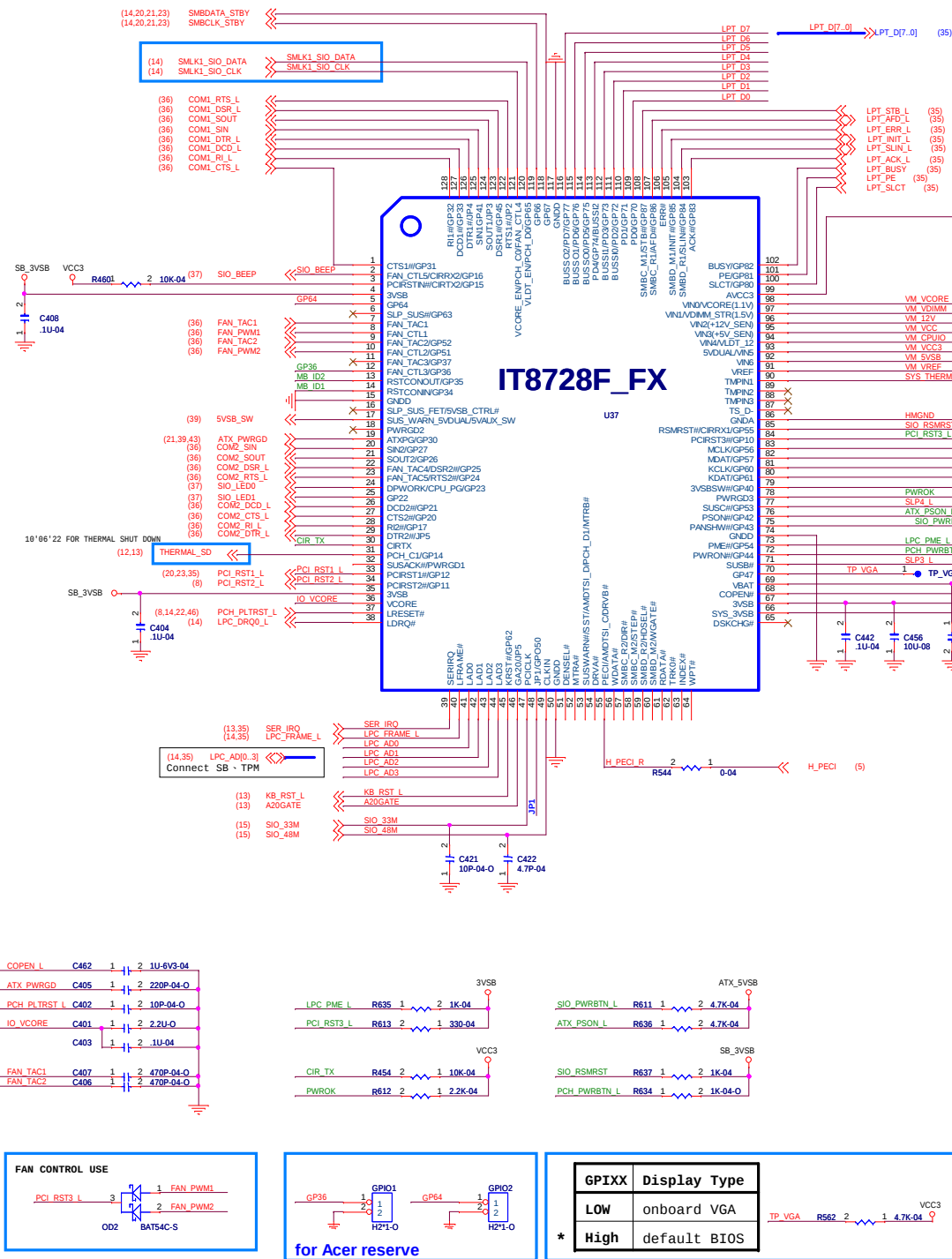
Close to Connector



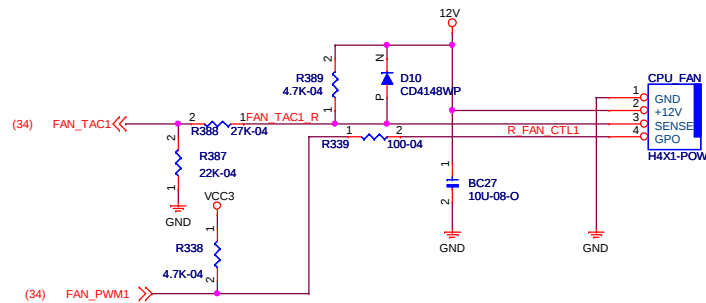
Close to Connector

**If build in Internal DVI Con,
that can use the circuit to protect reverse voltage together.**

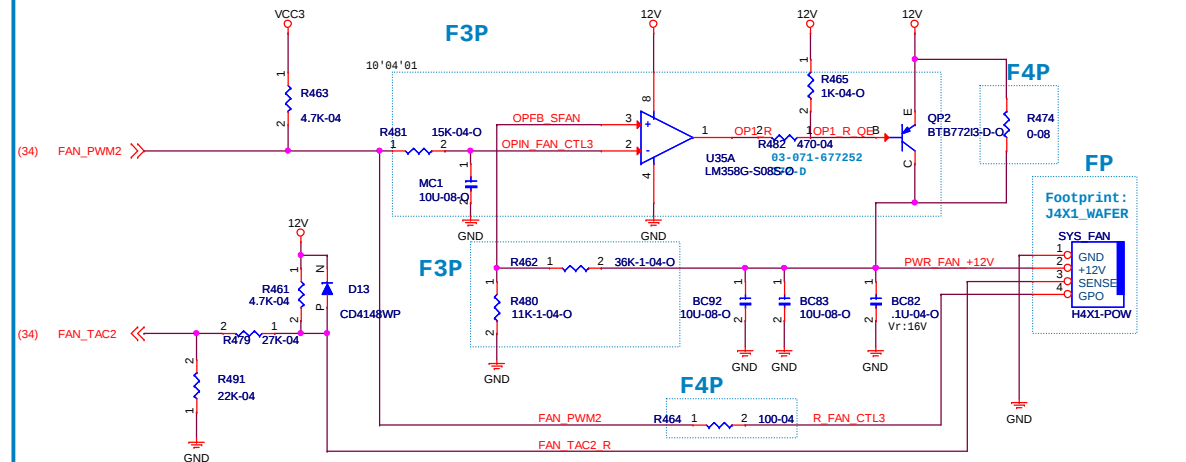






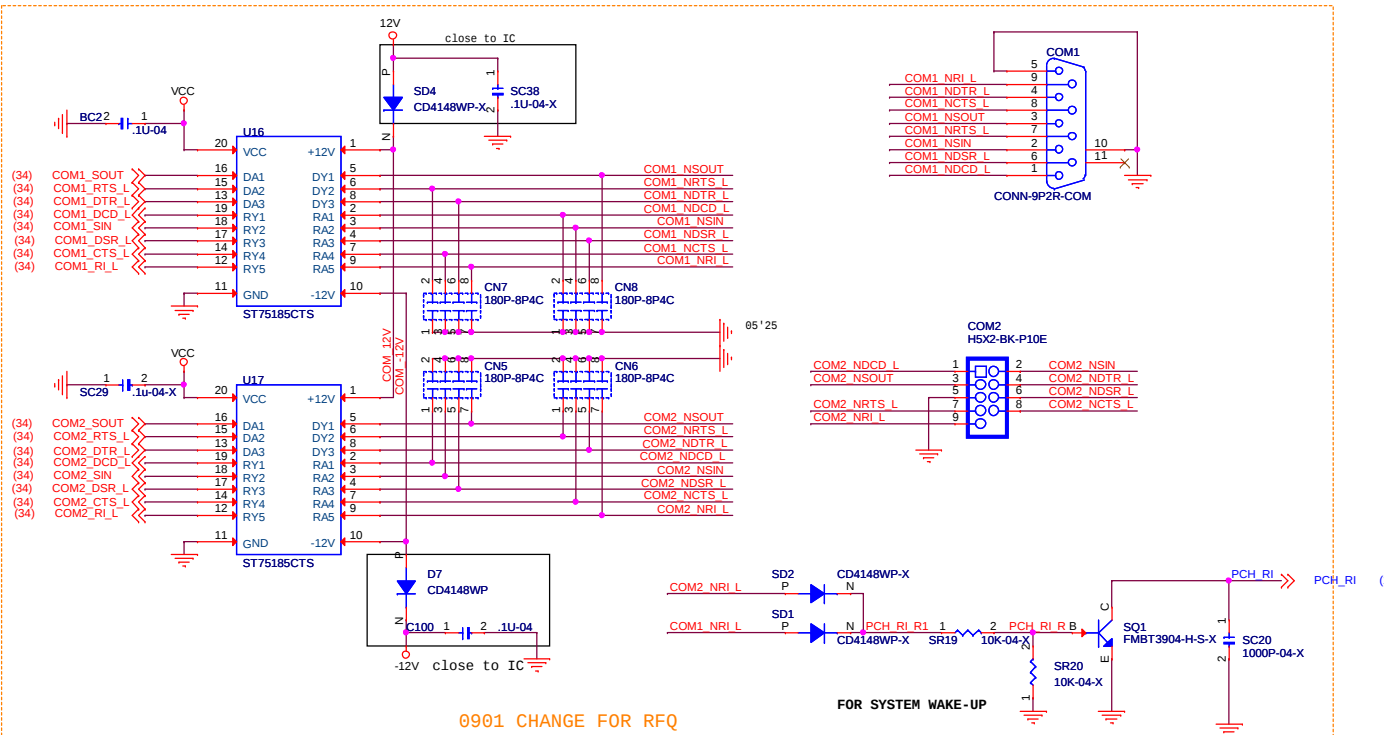


CPU FAN 4-PIN Circuit

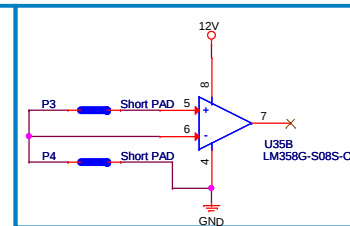


SYS FAN 3-PIN(Co-Lay 4PIN) Circuit

COM PORT I/O



0901 CHANGE FOR RFQ



PWR FAN:

MODE	F3P	F4P	FP Value
* 3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

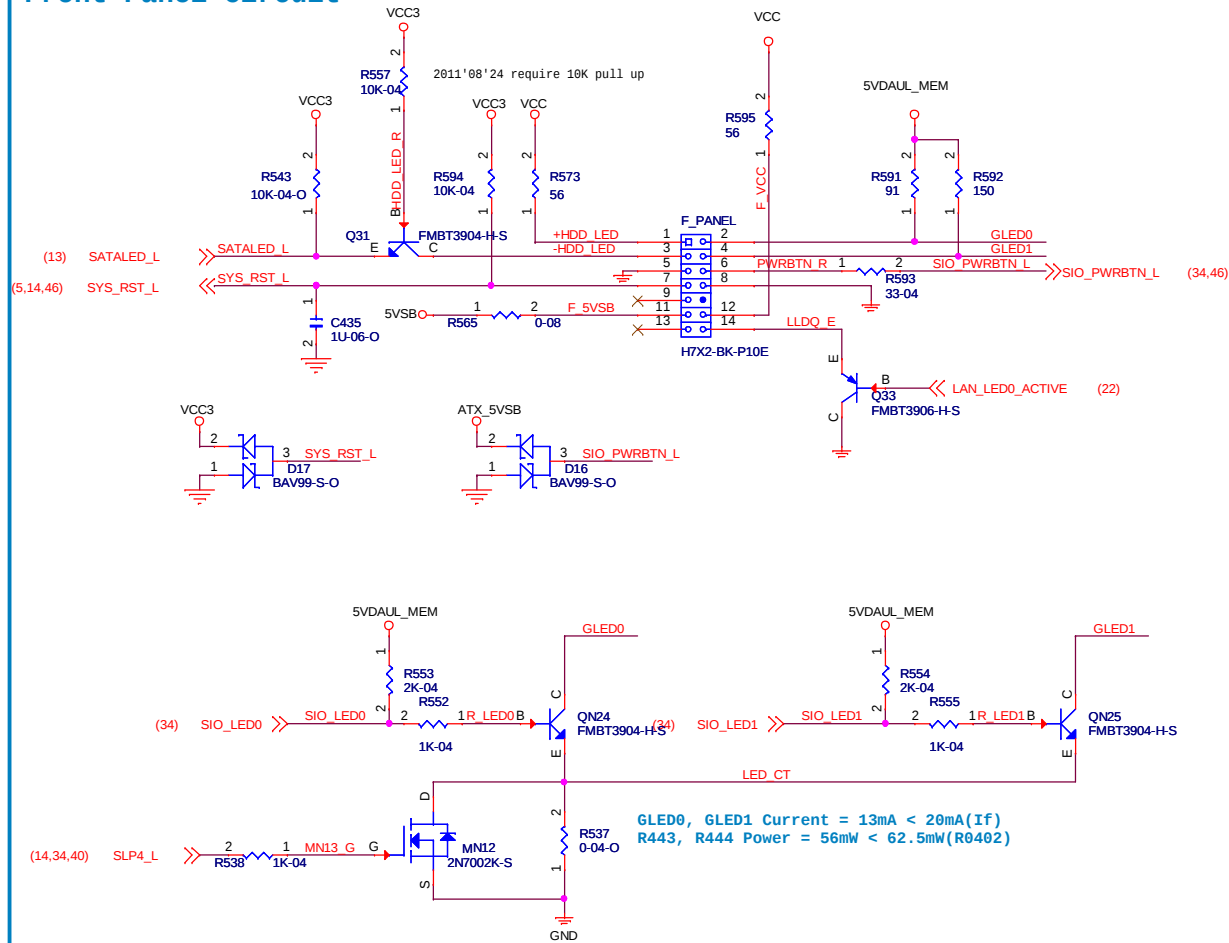
0901 CHANGE FOR RFQ

+ - terminal add short pad to ground for nonuse OP , 20110406

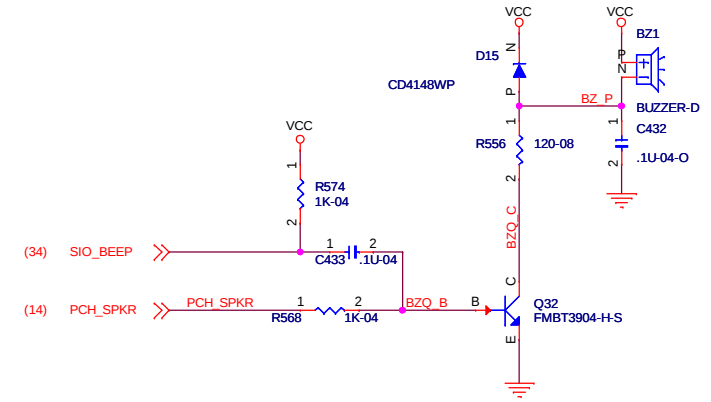
ECS Elitegroup Computer Systems

Title	FAN, COM	Rev	1.0.
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Front Panel Circuit

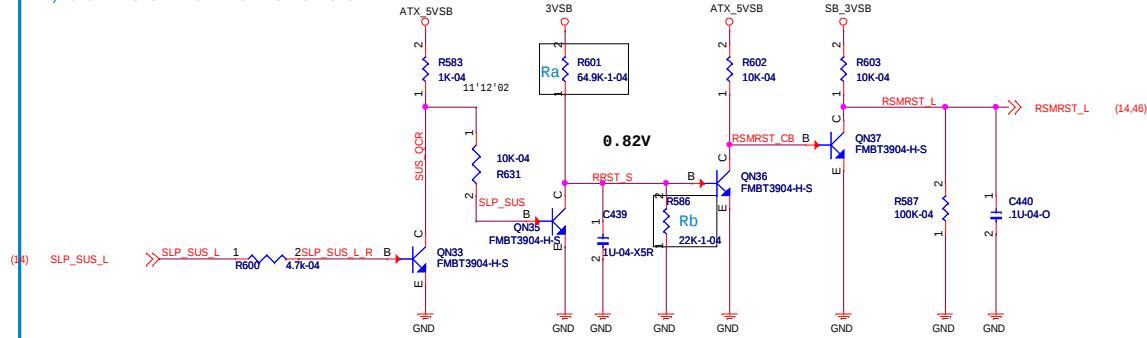


Buzzer Circuit

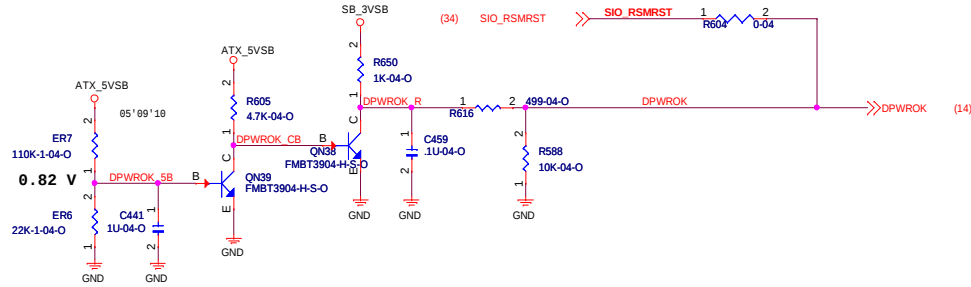


RSMRST Circuit

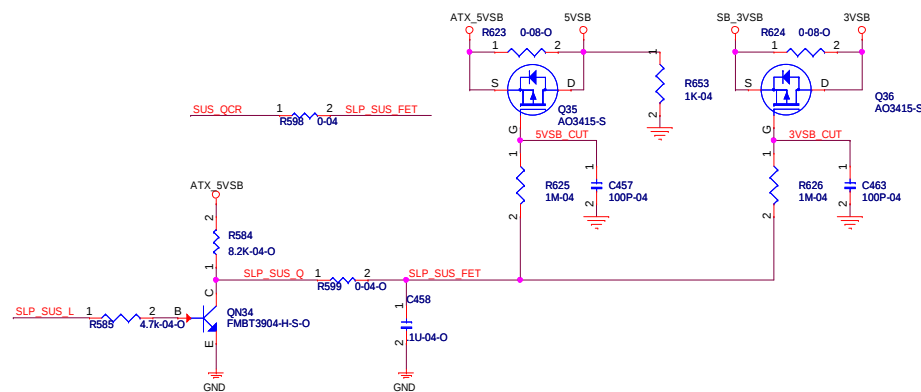
MODIFY Ra/Rb VALUE FOR FOLLOWING RULES
1)AC ON: 3VSB vs RSMRST(t₂₀₄: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V



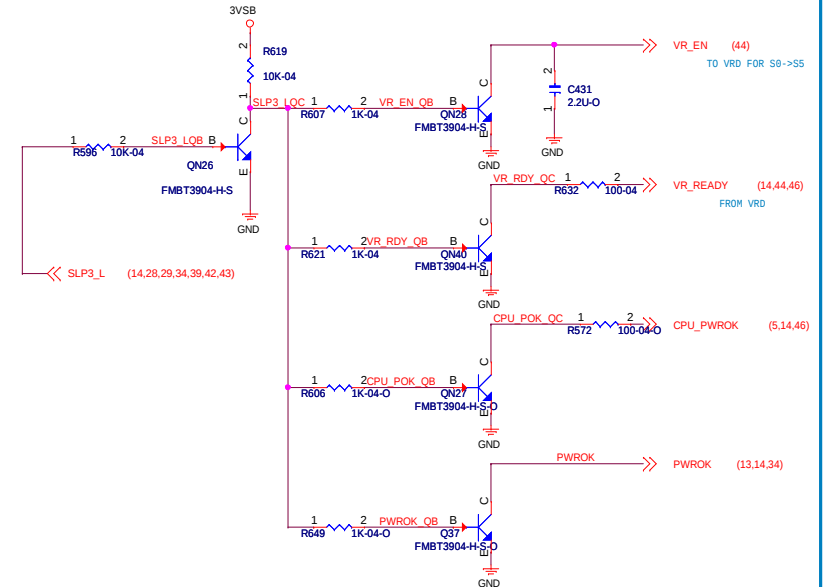
DPWROK Circuit



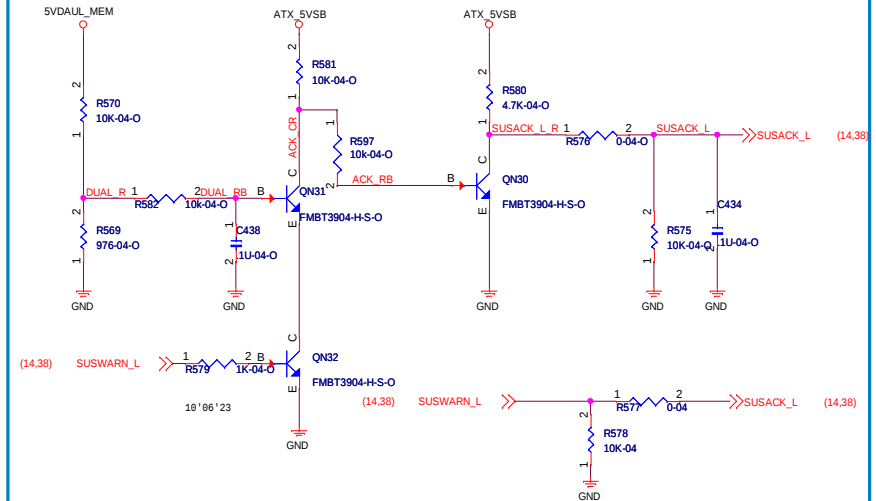
SUS_3/5VSB SWITCH



Power Down Sequencing Circuit



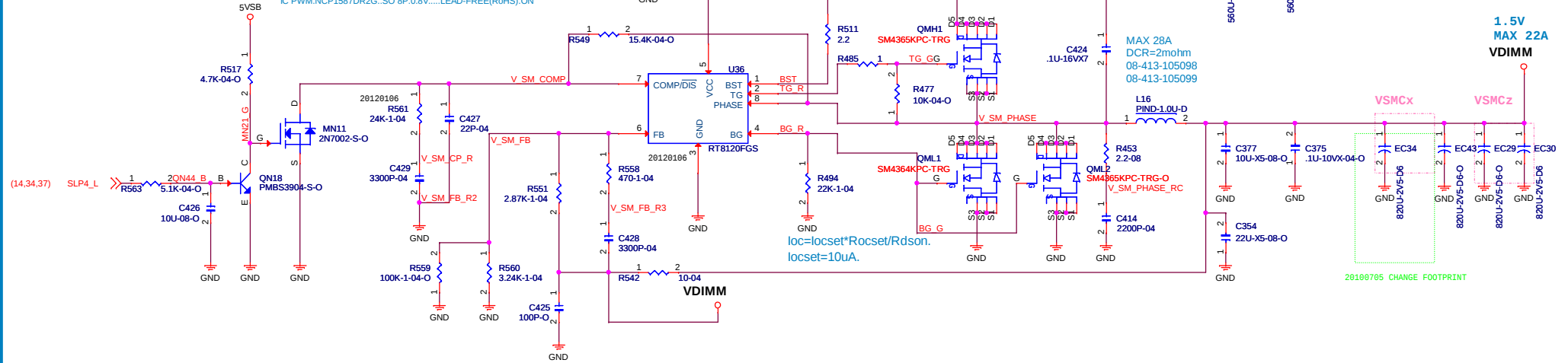
SUSACK_L CTRL CIRCUIT



VDIMM

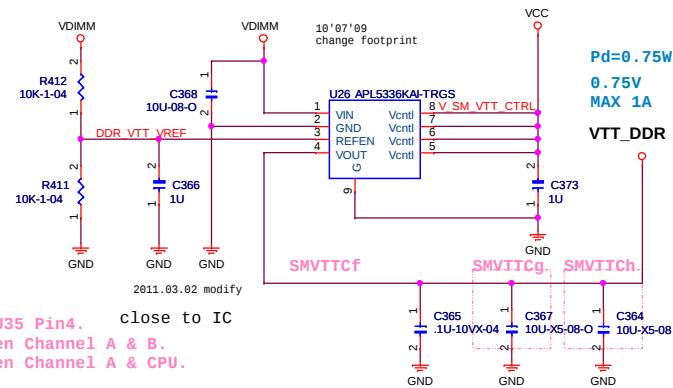
SLP4_L	High	Low
NCP1587DR26	Enable	Disable

NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS) ON



DDR_VTT

AP5336/GS9020/AME9172M



Elitegroup Computer Systems

Title	DC/DC VDIMM/DDR_VTT		
Size	Document Number	Rev	
Custom	Q77H2-AD	1.0	
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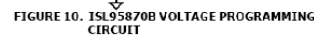
VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



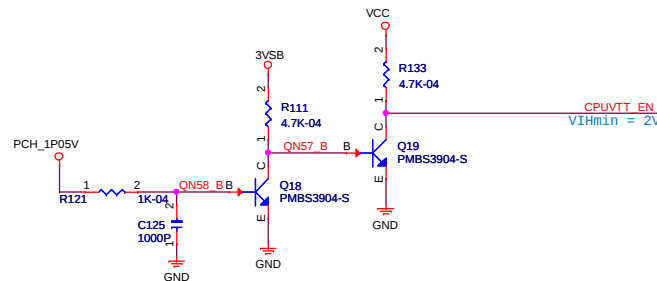
- I_{SS} is the soft-start current source at the 20 μ A limit
- V_{SREF} is the buffered V_{REF} reference voltage

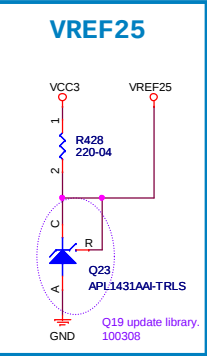
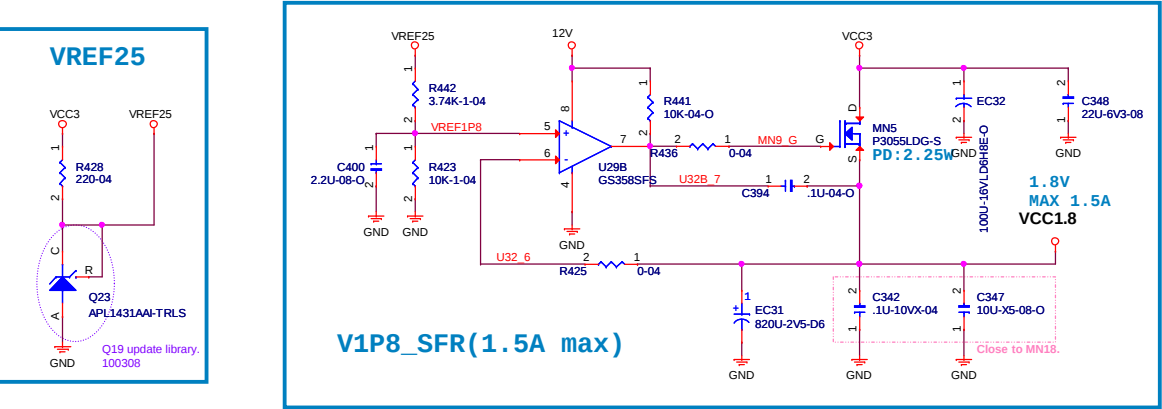
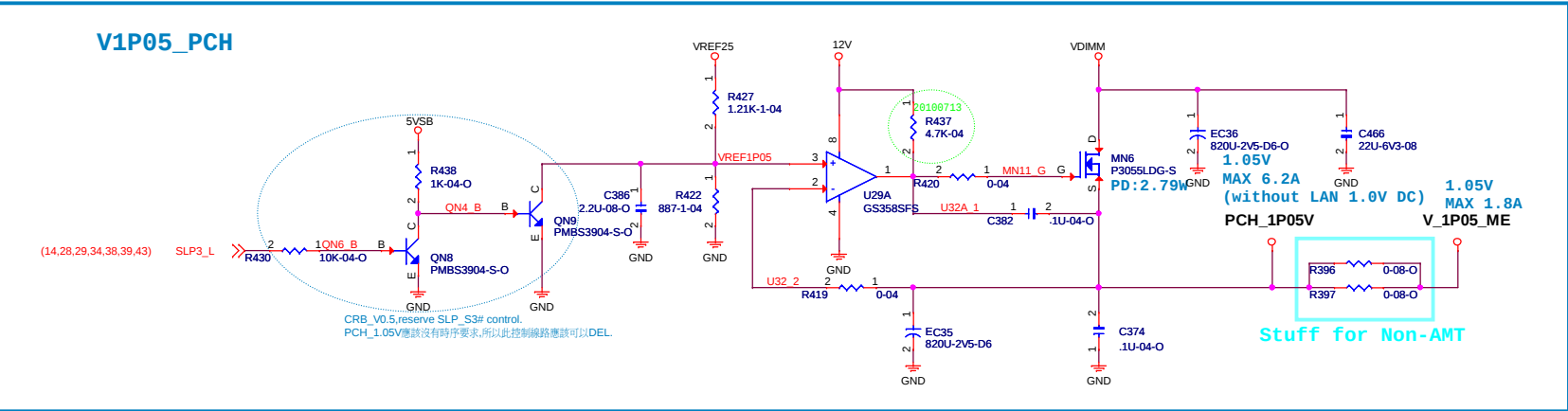
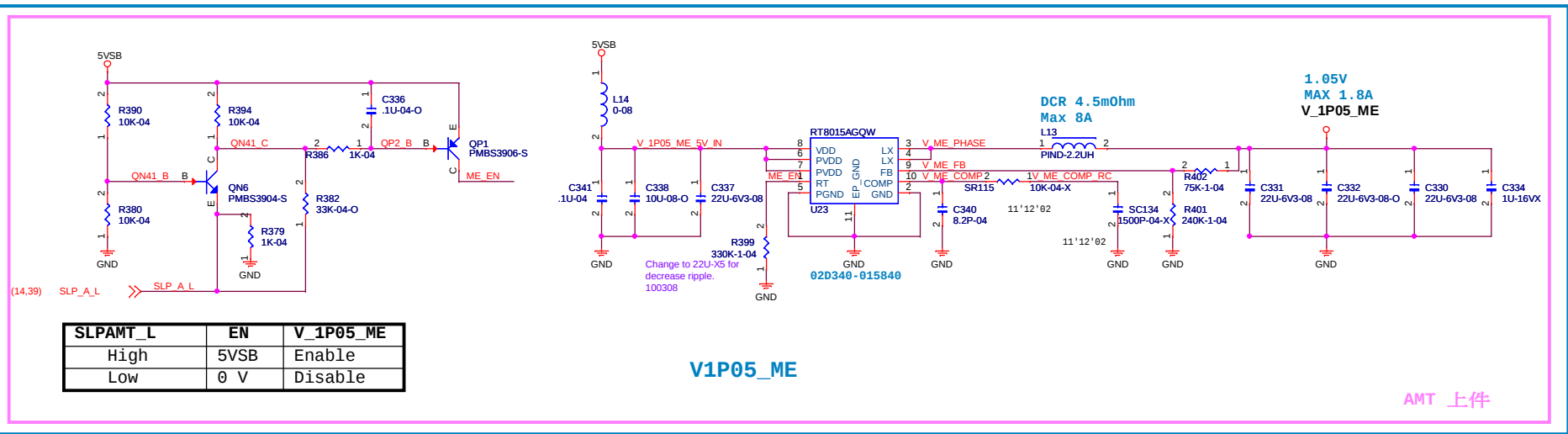
VID STATE		RESULT		
VID1	VID0	CLOSE	V _{SET}	V _{OUT}
1	1	SW0	V _{SET1}	V _{OUT1}
1	0	SW1	V _{SET2}	V _{OUT2}
0	1	SW2	V _{SET1}	V _{OUT3}
0	0	SW3	V _{SET4}	V _{OUT4}

The ISL95870B V_{SET4} setpoint is written as Equation 24:



Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC





Default Stuffed:

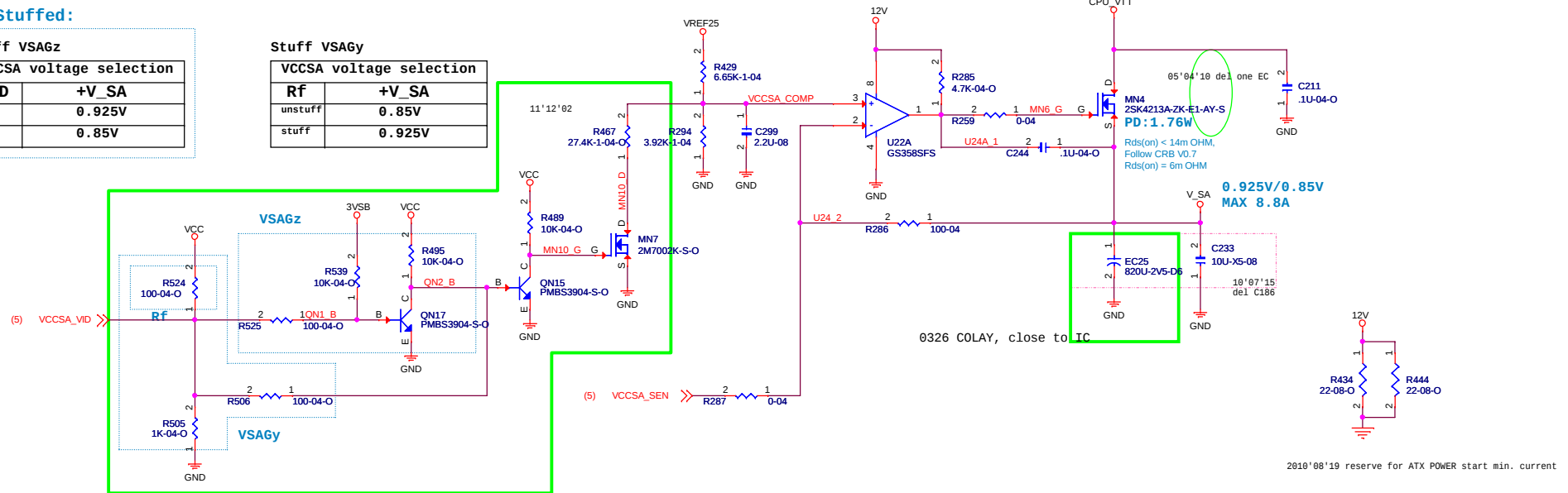
Stuff VSA6z

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*

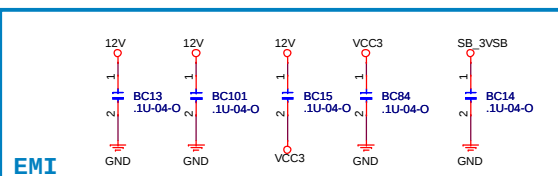
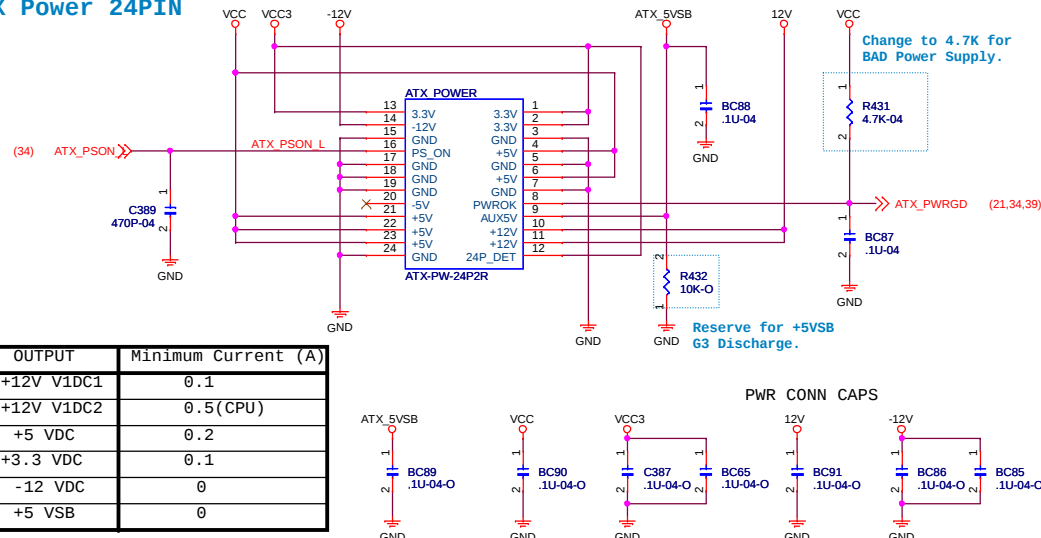
Stuff VSA6y

VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V

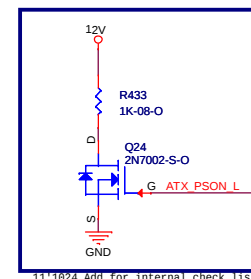
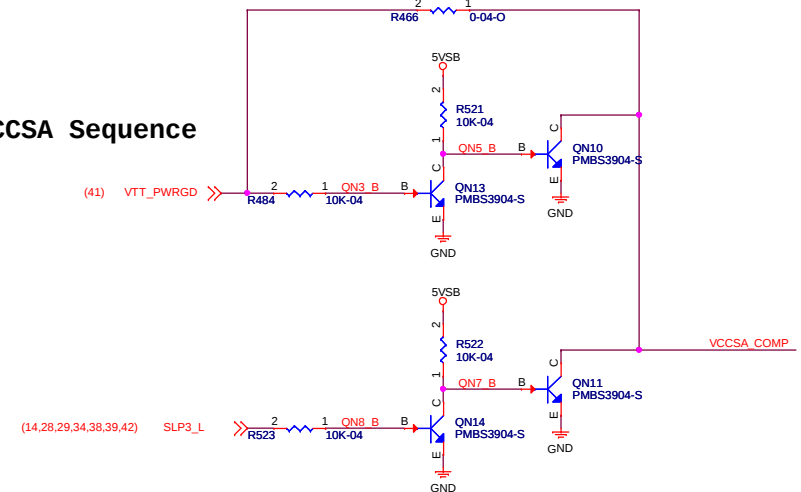


2010'08'19 reserve for ATX POWER start min. current

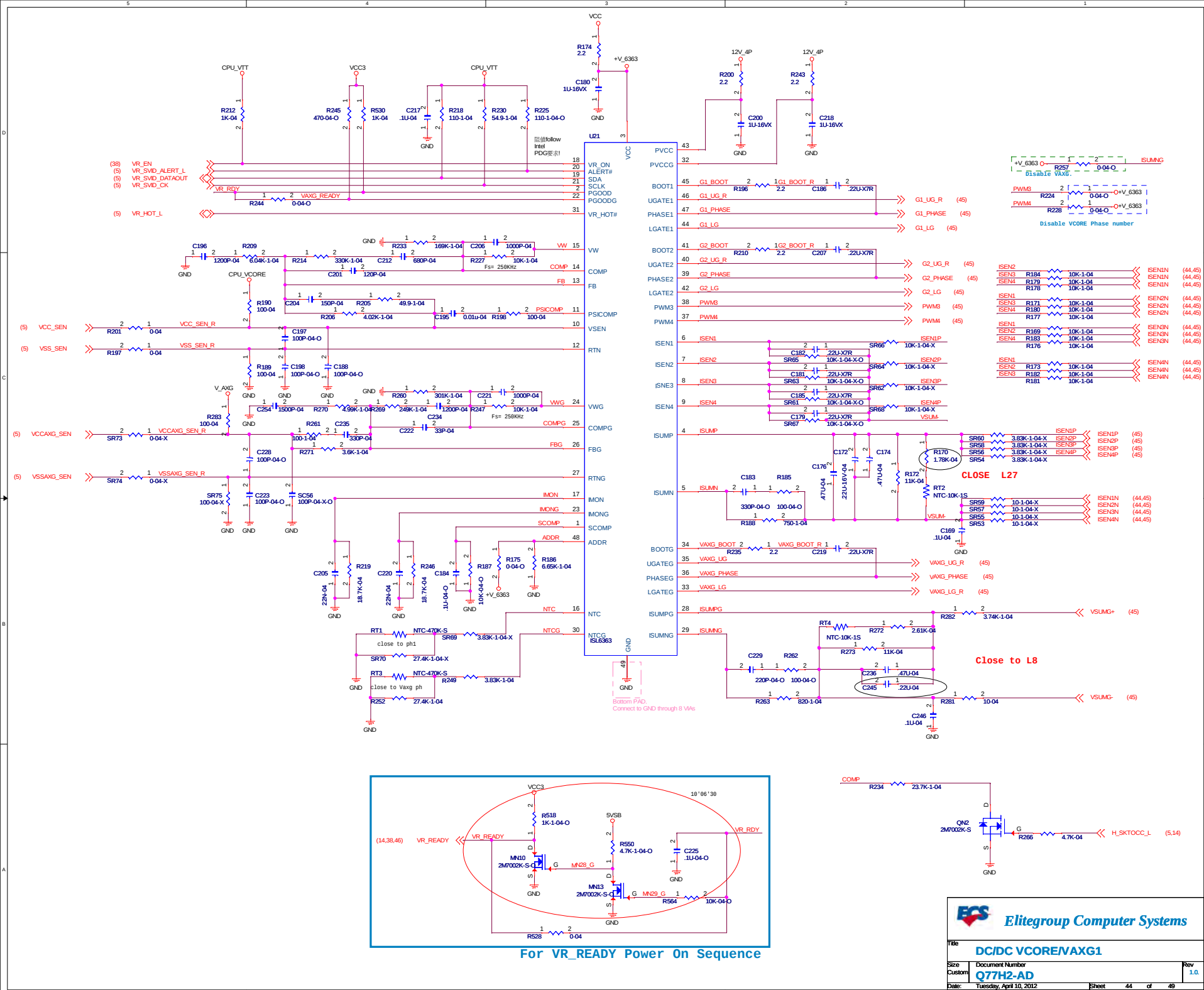
ATX Power 24PIN

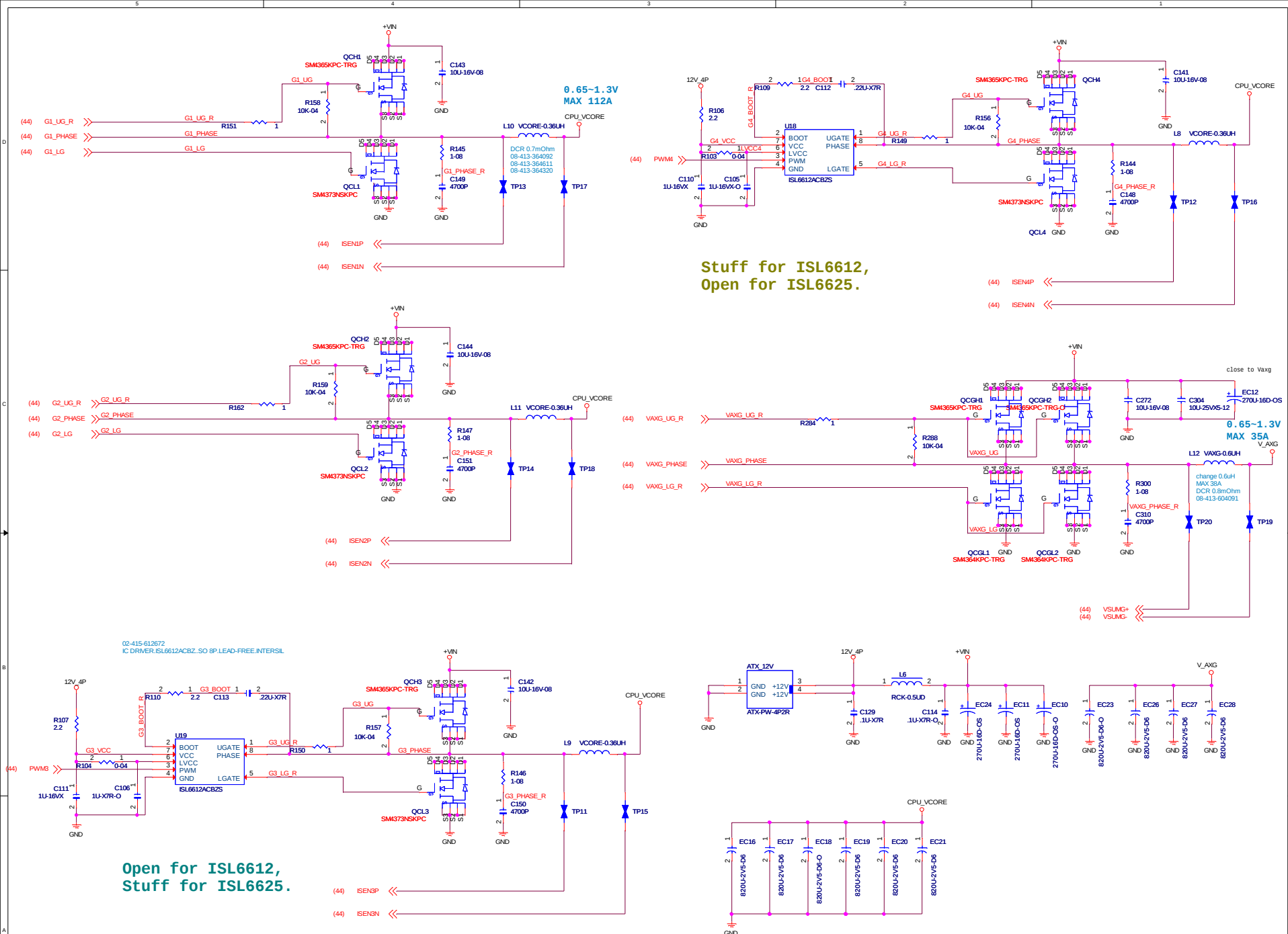


VCCSA Sequence



11'1824 Add for internal check list

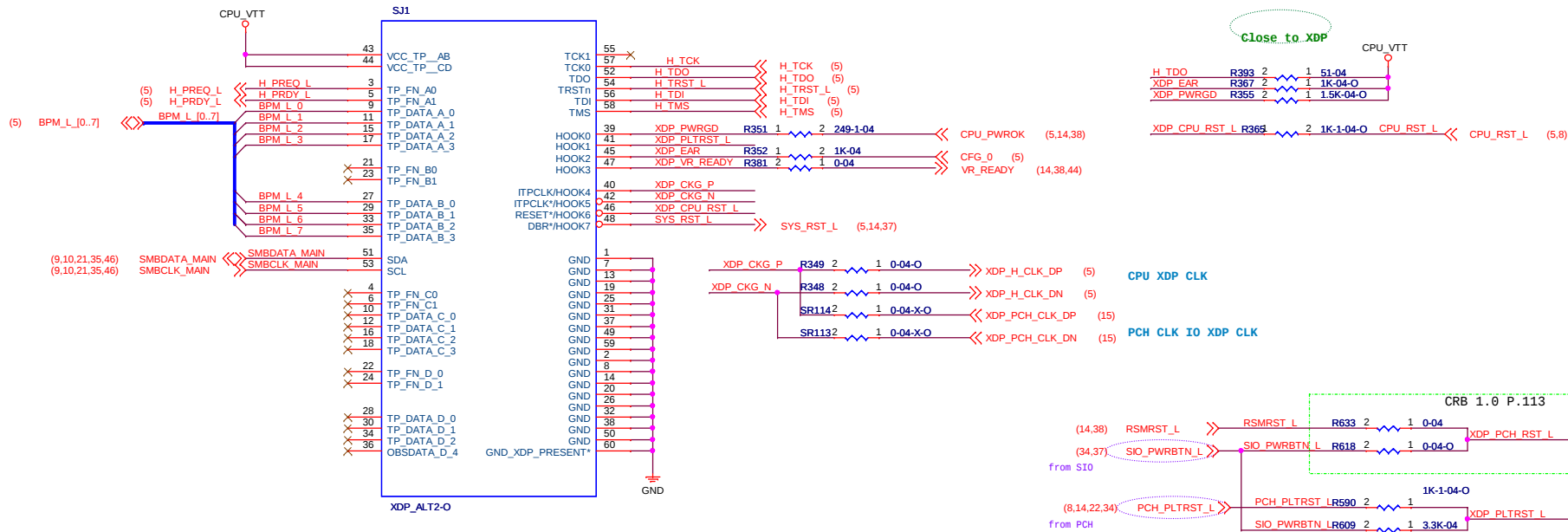




Stuff for ISL6612,
Open for ISL6625.

02-415-612672
IC DRIVER ISL6612ACR2S SO 8P LEAD-FREE INTERSIL

Open for ISL6612,
Stuff for ISL6625.



DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN

